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A Hybrid Real Time Locating System based on Inertial and RF Proximity Sensors

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GPS tracking and WIFI assisted LBS (Location Based Services) are today already available in outdoor environment and consequently there is a constant rising interest toward localization services in indoor environments such as airports, shopping mall, universities and generally in all the public and private closed environments where GPS signal is not available.

There are several techniques that can be implemented in such contexts, each with different approaches in terms of obtainable complexity and accuracy. WIFI fingerprinting techniques [1] usually require a prearranged planning stage and may suffer of poor accuracy, with experimentally obtained errors of several meters, depending on environments conditions.

The growth of computing power and the availability of modern hardware smartphone equipped with sensors such as accelerometers, magnetometers and gyroscopes can implement a location-based inertial systems INS (Inertial Navigation System) based on dead reckoning. In this case it is possible to estimate the current position from a previously known one, by exploiting a set of measurements made by inertial sensors IMU (Inertial Measurement Unit) [2-3]. In order to estimate the current position of the user terminal, it is necessary to know the distance and direction in a certain time interval, in addition to the starting point.

The main disadvantage of these techniques is that the integrating nature of the estimation is subjected to cumulative errors on the calculated position. For this reason, if the inertial system is used for long periods of time, it needs to be re-phased.

The dead reckoning based localization system, implemented in this work, uses the information obtained from the accelerometer sensor for the detection of the human steps; in addition a sensor fusion algorithm makes use of the magnetometer and acceleration values in order to estimate the direction of the target. The accuracy of the location with dead reckoning is therefore influenced by the efficiency in estimating the step and direction. The errors introduced by dead reckoning may be mitigated by using some proximity sensors (namely iBeacon) based on Bluetooth Low Energy (BLE 4.0) wireless communication. They periodically emit Bluetooth signals and allow the target, which is located within the respective coverage radius, to obtain and correct its position.

Some tests have been carried out with an Android OS smartphone, by experimentally measuring the localization errors calculated as the difference between the real and estimated positions of dead reckoning only method and with this hybrid approach just described (Fig.1). Comparative values of the localization errors are shown in Table 1. The hybrid localization in most test points has a location error less than the dead reckoning method, while the average error on all the 18 test points is of about 1.5 meters.

The proposed hybrid localization system, despite not using correlation methods with topological constraints or intensive computation based on Kalman filtering, allows a real time localization with an easy correction of the error introduced by dead reckoning. All the logic works inside a smartphone, so the presence of a remote infrastructure during the localization is not needed, while the use of integrative approaches could further improve the proposed system. Finally the proposed hybrid localization system is environmentally friendly since it uses technologies with very low electromagnetic pollution and low energy consumption.

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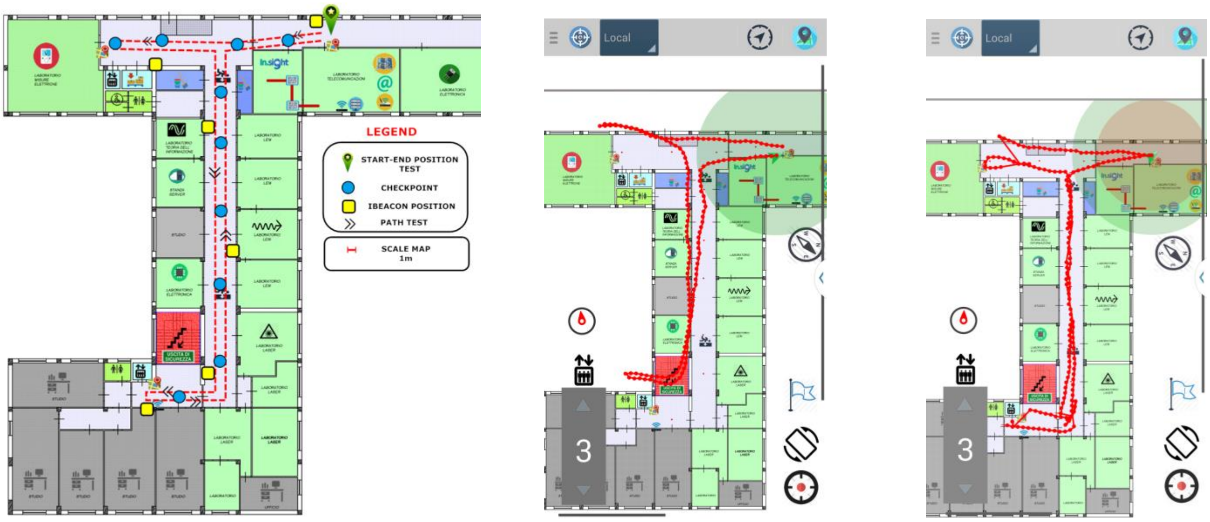

Figure 1: The figure on the left shows the planning iBeacon and the test area. The central and right figures respectively show the path of the target using the dead reckoning localization only and hybrid one.

Checkpoint	Dead Reckoning Error [m]	Hybrid Localization Error [m]
1	0.68	0.54
2	2.35	1.10
3	2.76	1.86
4	3.82	0.69
5	3.37	0.14
6	4.87	0.85
7	5.62	1.66
8	3.75	1.50
9	5.58	0.66
10	4.53	1.91
11	6.39	0.74
12	5.12	1.06
13	2.03	3.07
14	1.09	3.51
15	1.70	3.67
16	2.75	0.35
17	2.37	2.60
18	2.01	1.29

Table 1: Comparison of localization errors using dead reckoning only and the hybrid approach .

A Low-Cost, Open-Source Cyber Physical System for Remotely Controlled Agriculture

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This paper presents a low-cost solution for remote control of agricultural applications, a domain of growing importance. We propose the design of a flexible embedded system architecture able to support various kinds of remote control solutions. The goal is to enable the management of remote cultivations (in greenhouses and/or open-air) by exploiting sensors (e.g., temperature, moisture, radiometers, cameras) and actuators (e.g., motorized windows, irrigators, tools to deploy chemical products) directly through a smartphone app. This approach could allow controlling irrigation at different times of the day, optimizing fertilization and overall planning of the farming activity based on the actual weather and environment conditions.

The main innovation of this work consists in the fact that the platform is entirely based on low-cost electronic components assembled in open system architectures. These architectures, typically based on the Arduino and Raspberry platforms, have become ever more popular and embedded systems are being built based on them in several application areas. Moreover, they are well supported by active communities of developers.

The overall system architecture is represented in Fig. 1, where we can identify the three main architectural layers: a smartphone app, for user interaction, a central unit (CU) for overall coordination and a set of devices deployed in the field.

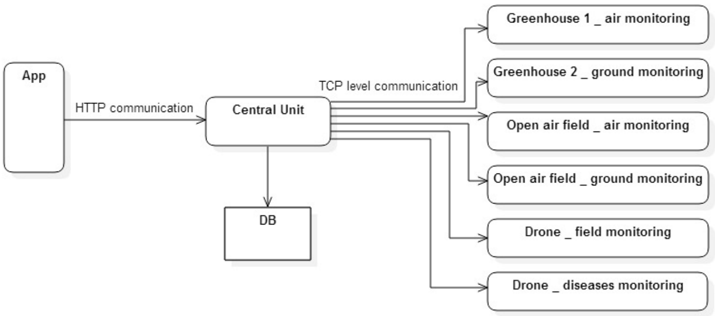

Figure.1. System architecture, with the app, the central unit and the field devices (on the right).

The above mentioned three layers implement three different decision levels. The first one, the tactical level, is a closed-loop cycle on the controlled variables and allows the field devices to tune up actuators according to the detected context. Examples concern the control of temperature ranges and of activity time, in order to give advices to the farmer. The strategic level allows the CU to perform multivariable analysis coordinate and control the activities of various field devices, also exploiting Artificial Intelligence. The operational level is implemented in the smartphone and allows the farmer to control the whole system, also blocking or activating automatic controls, if necessary.

The main responsibility of the field devices is to sense physical quantities from the environment and run actuators. They communicate with the CU, receiving instructions and delivering results. The field devices are based on Arduino Uno equipped with Ethernet shield, LCD Display and other specific sensors/actuators depending on their specific task. They are programmed in the C-like Wiring language. Figure 2 shows the field device loop, sensing context data and answering to the client requests.

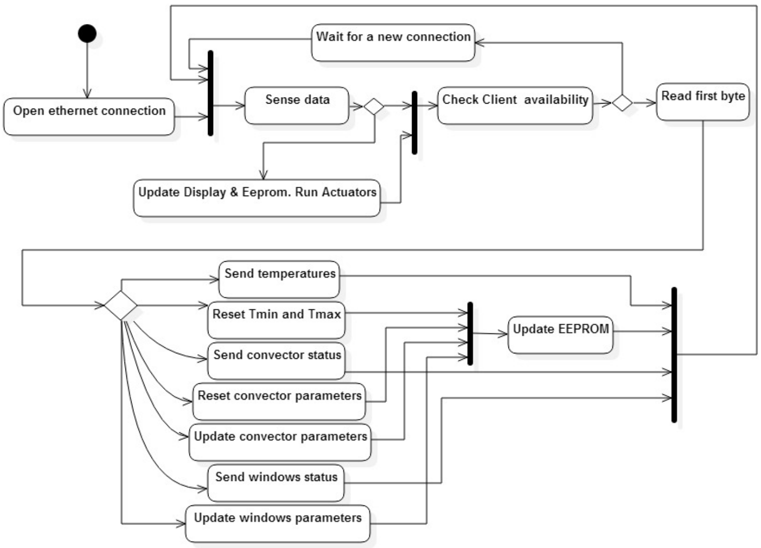

Figure.2. Greenhouse device behaviour. The field device performs the loop, sensing data and answering client requests.

The Central Unit (CU) manages all the communications between the two peripheral systems and hosts a DB for logging and statistics. It is based on Raspberry hosts some servlet classes, managed by the Tomcat servlet container. The database is MySql and accessed through the JDBC libraries. The CU runs an infinite loop that updates the database and performs control activities.

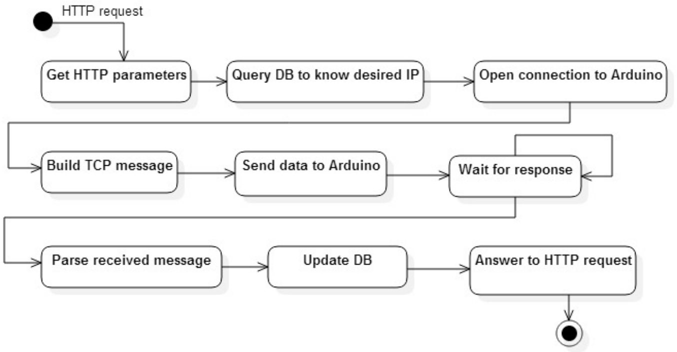

Figure.3. Central unit behaviour. Following the http requests, the central unit interacts with the DB, communicates with the field devices and finally answers to http requests.

The smartphone app allows the farmer to command the field devices through a pleasant user interface, which supports the organization of the work. The app is currently implementation on a Windows phone, with logic programmed in C# and graphics described in XAML.

Results are still qualitative, and concern the validation of the functioning of the system, that has been achieved through the test of all the functions exposed by the system through the mobile app. The list of the functionalities includes: request of the status of the temperature sensors; update of the sensors' temperature thresholds; reading, recording and resetting the minimum and maximum temperature values; request of the status of the windows; request of the status of the heating system (also including activity length); request of immediate take-off of the drones, with related flight-path instructions.

The most interesting result of the proposed system consists in its versatility. In particular, the system is easily extensible by plugging different field sensors (open and closed environment, drones for monitoring and for spraying fertilizers, etc.), that can be seamlessly integrated by reconfiguring the CU and the app.

A Novel Architecture for Real-Time Space Variant Image Deconvolution

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Deconvolution of an image is a very useful process adopted in several applications, for instance to retrieve the information content or the details originally present in an image, when it has been corrupted by blurring. This can happen for example when the image has been acquired through low quality optical systems or when the camera shake or a movement of the subject, during the open shutter time, create some blurriness [1,2,3,4]

It is not always possible to exactly invert this process, but a maximum likelihood solution can still provide good results. Lucy and Richardson in particular have developed an iterative algorithm (LRA) that after some tens of iterations provides appreciable results [5,6].

In real cases the system to invert typically presents a space-dependent impulse response, i.e. a different point spread function (PSF) for each pixel of the image, consequently its representation is extremely memory demanding. In these cases LRA, although theoretically correct, is extremely difficult to apply due to the huge resources required and also to the long computation time.

In this work we have proposed an architecture, suitable for an FPGA implementation, able both to contain the required resources and to parallelize the processing flow. The entire iterative deconvolution algorithm has been estimated to be able to run in real-time adopting medium quality images (640x480) with a frame rate of 5 fps, acceptable e.g. for video surveillance systems.

The strategies adopted to ensure the feasibility of the system and to guarantee the real-time performances are essentially two:

1- Reduction of the resources required to model the convolution process by adopting a suitable coding to describe and store the PSF associated with each pixel of the image, through a suitable encoding/decoding algorithm.

2- Realization of a parallel architecture suitable to split the image convolution operation in tens of channels operating in parallel. The proposed architecture takes also advantage of the facility of the FPGAs to store image data exploiting hundreds of memory blocks (BRAM), which can be accessed in parallel without any conflict.

The architecture developed in this work is highly scalable and can be used for other kinds of algorithms where fast images convolution are required.

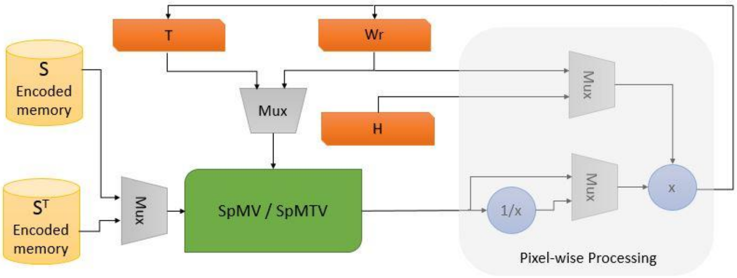

Figure 1. The architecture proposed to simplify the realization of the iterative convolution process addressed in the Lucy-Richardson algorithm

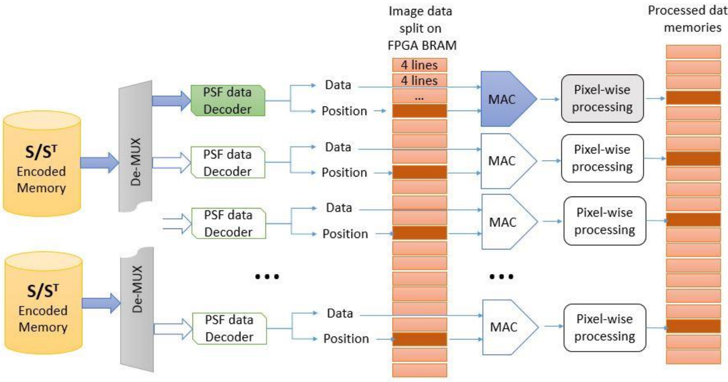

Figure 2. The structure of the proposed architecture designed to speed up the space-variant convolution process using several channels working in parallel.

.. (a) (b)

Figure 3. (a) Representation of the PSFs matrix. (b) Simulated results: an original frame (left), its corrupted version (center), the restored frame (right).

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A smartphone-enhanced pill-dispenser as an example of mHealth application

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Healthcare has deeply changed in the recent past thanks to the continuous improving of electronic devices and the advent of affordable and ubiquitous communication technologies. For example, the term mHealth refers to the practice of medicine and healthcare supported by mobile (smart)devices. The growing importance of mHealth is also confirmed by the announcement, on May 2014, of the “Simband” and the “HealthKit” projects by Samsung and Apple, respectively. Possible advantages include a reduced hospitalization time and better home-based rehabilitation. In addition, the availability of an immediate feedback for the patient, also allows for a better self-management of the daily care. In this abstract, a smart pill-dispenser is described as an example of mHealth application. Authors mainly focus on the low-cost requirement, in order to overcome one of the limitations of currently available devices. The novelty of the proposed approach is the adoption of a smartdevice not only for providing a user-friendly human-machine interface, but also for the automatic identification of the patient (a feature particularly important for elderly). The developed solution embeds a supervising microcontroller and uses the short-range Near Field Communication (NFC, in particular the so called Reader/Writer modality, allowing the smartdevice to behave as a regular RFID tag reader) wireless link to exchange data with the smartdevice. In addition, the user actions are monitored as well, in order to infer and log in-take activity.

The NFC is based on the physical layer of widely diffused High Frequency RFID, operating at 13.56MHz, allowing an operating range on the order of few centimeters. A variety of NFC standard stacks are defined, offering different modulation schema, bitrates and message formats. Among all of them, the NDEF format is used in this work, based on the ISO14443-4A specification. In particular, a proprietary application level protocol has been purposely designed and encapsulated within NDEF messages. In order to test interoperability, two smartdevices have been considered: a smartphone, Samsung S4 Mini (GT I9195), running Android 4.2, and a tablet, ASUS Nexus 7 (2012), running Android 4.4. The microcontroller based pill dispenser (hosting a Microchip PIC24F), gains NFC functionality via a low cost AS3953 by AMS. The proprietary application level handles commands/responses encapsulated into NDEF messages. The microcontroller firmware is complemented by an Android app purposely developed. The firmware occupies less than 15 kB of µC code space and the Android app occupies about 1.5 MB of smartdevice internal memory.. A test bench has been assembled to demonstrate the feasibility of the proposed approach and to evaluate overall system potentialities in terms of communication delays (evaluating time elapsed between the passively energizing of AS3953 and the reception of an NDEF message by µC) and jitter (evaluating system behavior on periodic message communication).

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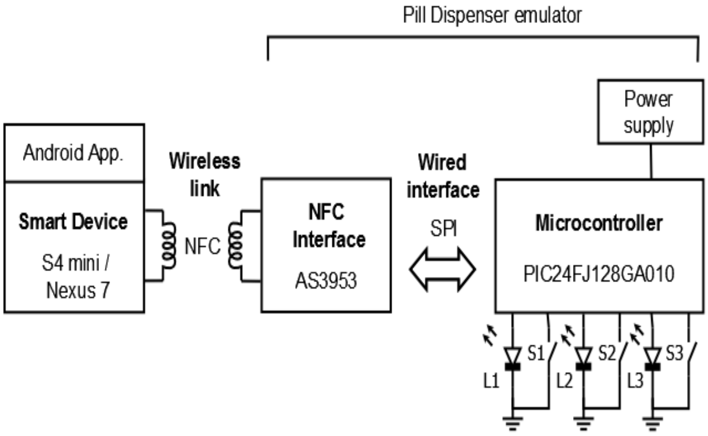


Figure 1: System overview of the proposed smart pill-dispenser.

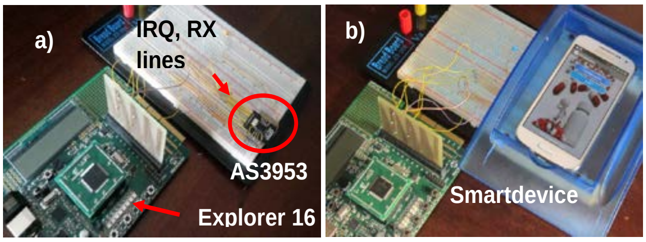


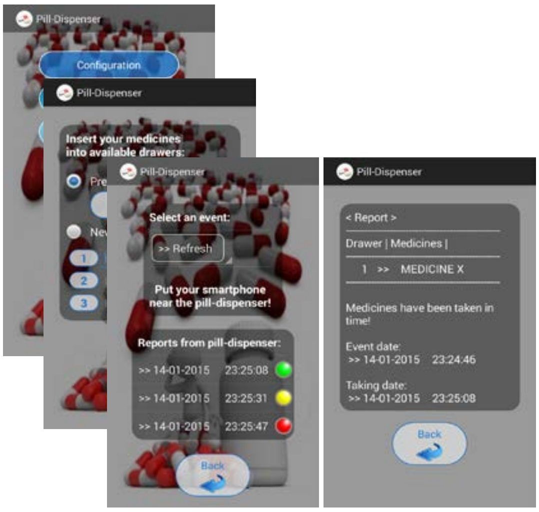
Figure 2: Real-world prototype; a) NFC device highlighted; b) the whole system including the smartdevice.

TABLE I. LATENCY MEASUREMENTS.

	S4 mini		Nexus 7	
Latency	**848 kbps**	**212 kbps**	**848 kbps**	**212 kbps**
Mean [ms]	538.30	572.40	511.90	548.90
Std. Dev. [ms]	49.10	41.00	135.23	168.66

Tests conditions are the following:

- The smartdevice is approached and wirelessly powers the AS3953 module, which sends a power-up interrupt request to µC on IRQ line.
- The smartdevice sends an NDEF message to the AS3953 module and µC RX line is toggled when the reception of the message on µC is completed.
- The time elapsed between first interrupt request on IRQ line and the RX line toggling is measured.



Insert your medicines into available drawers:

Select an event:

Put your smartphone near the pill-dispenser!

Reports from pill-dispenser:
>> 14-01-2015 23:25:08 🟢
>> 14-01-2015 23:25:31 🟡
>> 14-01-2015 23:25:47 🔴

Drawer | Medicines |
1 >> MEDICINE X

Medicines have been taken in time!

Event date:
>> 14-01-2015 23:24:46

Taking date:
>> 14-01-2015 23:25:08

Figure 3: Screenshots of the developed Android application.

TABLE II. JITTER MEASUREMENTS.

	S4 mini		Nexus 7	
Jitter	**One App**	**Ten Apps**	**One App**	**Ten Apps**
Mean [ms]	1002.10	1003.20	1000.50	1001.20
Std. Dev. [ms]	7.72	20.72	3.77	5.86

Tests conditions are the following:

- The smartdevice executes a 1s-interval periodic task. Within this periodic task, the smartdevice sends an NDEF message to the AS3953 module.
- When each message reception on µC is completed, µC RX line is toggled.
- Half-period of resulting square wave on RX line is measured.

Jitter measurements performed for different CPU loads

A voltage mode interface for biomimetic differential capacitive flow-sensor arrays

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Differential capacitive sensors are capacitive half-bridges where one capacitor has positive position dependency and the other negative. In other words, the capacitance values change either in the same or in a complementary way in respect to a stimulus that can be, for example, a movement. The employment of a differential capacitive structure helps to reduce resolution problems related to low capacitive variations and common mode disturbs [1]. This capacitive modelling can be applied to a plate distance sensing system, where the series of two capacitors are formed by two fixed plates and one movable in the middle, which changes its position from its nominal one owing to the sensing effect. Capacitive variation is related to the following sensor parameter changes: permittivity, distance between two capacitor plates/electrodes, one electrode deformation, etc.. For example, in hair flow motion detection, capacitive sensors with suitable electrodes (e.g., three electrode systems) can be employed for non-contact revealing of angles, reduced and higher displacements (by the detection of spacing and an area variation) and plate distance. This capacitive modelling can be applied to a three-plate distance sensing system, where the series of two capacitors are formed by two fixed plates and one, movable in the middle, which changes its position from nominal one owing to the sensing effect (Fig. 1) [2]. We have analysed two possible case studies, defining x as a dimensionless variable relative to the sensor measurand variations. Firstly, considering the areas of the capacitor plates changing linearly with x, C_1 and C_2 capacitances can be expressed according to eq. (1). On the other hand, if the distance between the electrodes is changing linearly with x, C_1 and C_2 have hyperbolic variations with x expressed as in eq. (2):

$$C_{1,2} = \frac{C_0}{2}\left(1 \pm x\right), \qquad (1) \qquad\qquad C_{1,2} = \frac{C_0}{2}\frac{1}{\left(1 \mp x\right)}, \qquad (2)$$

being C_0 the total capacitance of the transducer. We can notice that the measurand x can be expressed as independent from C_0 value, being, in both the cases (1) and (2) :

$$x = \frac{C_2 - C_1}{C_1 + C_2}. \qquad (3)$$

We here propose (see Fig.2) a novel interface that can be implemented either with discrete element components or in an integrated version, in a standard CMOS technology, the latter for low-cost integrated portable applications. The core of the interface circuit is composed by an integrator (A_2,R_3,C_1) and a differentiator (A_3,R_4,C_2,C_3) including the two capacitors of the sensor. These two cascaded blocks allow to obtain the relationship between the output voltage and the measurand, while comparator (A_1,R_1,R_2) is used to sustain the oscillation itself.
Referring to Fig.2, we can write:

$$V_{out}^{\max}\left(x\right) = \frac{R_4}{R_3} \cdot \frac{1+x}{1-x} \cdot V_{SAT} \ , \qquad (4)$$

being V_{SAT} the op-amp saturation supply voltage. Op-amp non idealities can be considered negligible. Concerning the sensor, we have considered a biomimetic hair flow sensor [3], having a C_O of about 25 pF and a relative variation of ±7.5 pF. Fig.3 shows the output voltage vs. the measurand *x*. Theoretical, simulated (through Orcad-Spice software) and experimental (measured) results are in a good agreement. Relative percentage error is very low between theoretical and simulated results (< 2%) and also between theoretical and measurements (< 3.5%). These results have been obtained employing a discrete-element board where R_1=R_2=R_5=R_6=100 kΩ, R_3=1.2MΩ, R_4=475kΩ, C_3=3pF, while LF411 has been chosen as operational amplifier (saturation voltage ≈ 9.14 V). Recently, a suitable Operational Transconductance Amplifier (OTA) has been developed as active block, so to have a complete integrated solution. Preliminary simulations had given satisfactory results also for this version of the interface. Sensitivity values, concerning the distance variation of the capacitance, are in the range 6-20 mV/µm, while resolution is between 23 and 83 nm [4].

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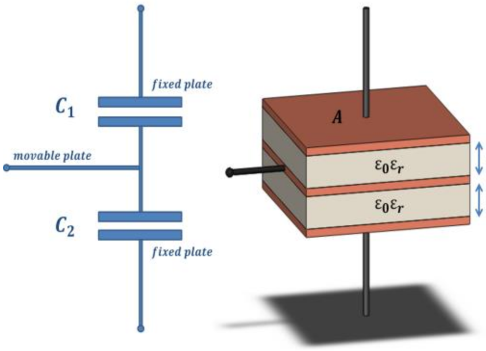

Figure 1: Differential capacitive sensors and its physical overview.

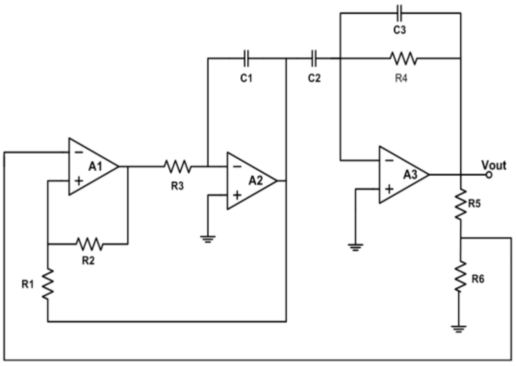

Figure 2: The proposed voltage mode interface (C1 and C2 form the differential capacitive sensor)

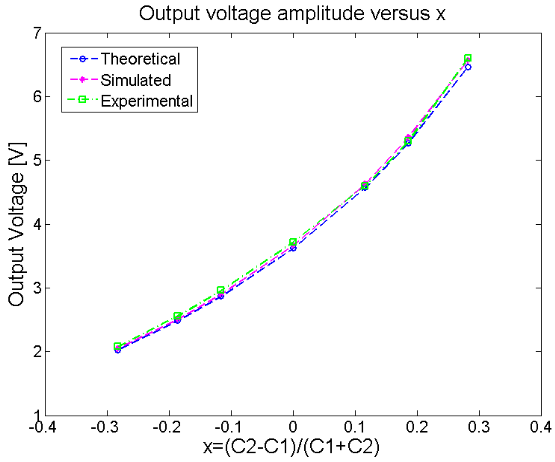

Figure 3: Output voltage vs. *x* variation.

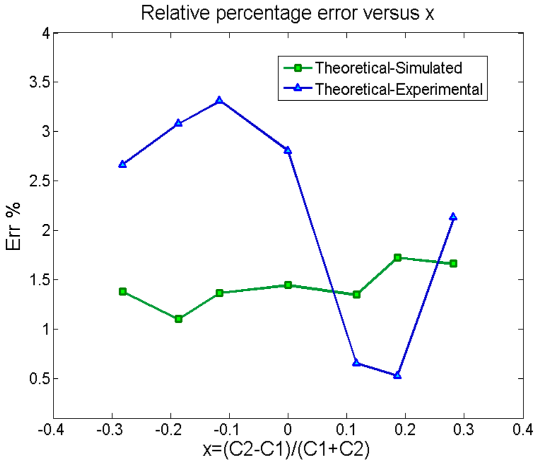

Figure 4: Relative % error vs. *x* variation.

Adaptive Custom Electronic System to Optimize Interconnections of PV Modules

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The increasing energy demand as well as the improved performance of solid state relays technologies that will be soon available at reasonable prices, let us imagine that the photovoltaic generation plants reconfiguration will be a realistic perspective. When one or more PV modules, belonging to a set of series-connected modules, are shaded, the maximum generated current gets reduced, decreasing the output power [1-2]. Dynamic reconfiguration can improve power output by reducing electrical mismatch conditions due to partial shading on some panels. In this way, roofs showing one or more obstacles will probably become a possible installation site [3].

Many topologies can be considered to perform reconfiguration. The most common, in existing PV generation plants, is Series Parallel. Using this topology, reconfiguration aims to build strings of series-connected modules that show similar irradiance levels. As a result, well-irradiated panels will not be limited in current by a less irradiated panel on the same string.

In order to test the effectiveness of the reconfiguration approach, a custom electronic system has been designed and implemented (Fig. 1). The Reconfigurable Solar Array System consists of different circuit blocks: a measuring system, a control logic, a switching matrix, supply and load. In a PV module, the irradiance level can be estimated by measuring the open circuit voltage, knowing physical parameters of the module and assuming that the cell temperature is the same for all modules, as shown in [4]. From this information, it is possible to reconfigure PV modules aiming to reduce the electrical mismatch among the modules of a same string.

Nine PV modules (see Table 1), made by BP Solar, have been used in our tests. The switching matrix allows to connect each module to whatever of the other eight modules, arranging them in three strings of three modules. These strings are then connected in parallel.

Some tests have been carried out during daytime. Starting from the configuration with all panels correctly working and shading one panel per string, the system reconfigures the connections between the panels. A suitable load was then chosen in order to allow the whole system to work in the zone of the PV characteristic where they act as voltage generators. With shaded panels, the test results show a substantial improvement between the power obtained with default configuration and that obtained with reconfigured panels. The results are shown in Table 2.

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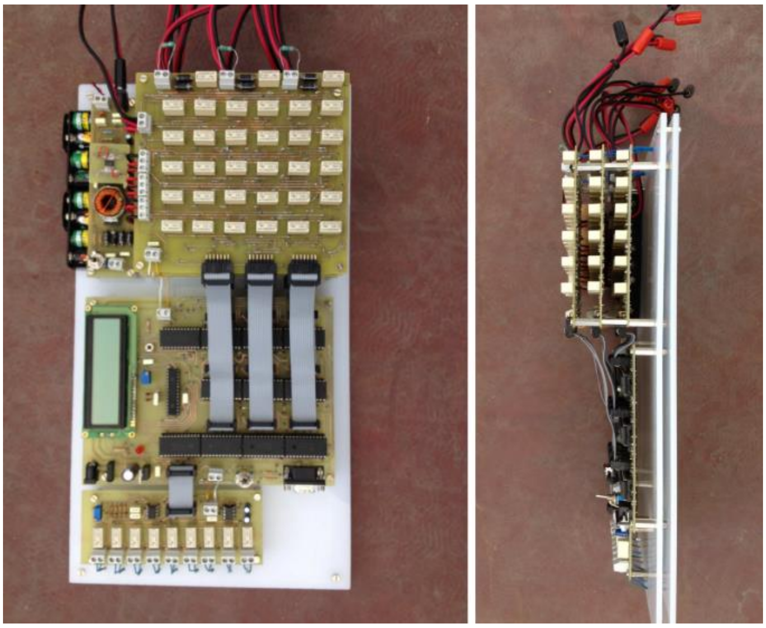

Figure 1: Simplified scheme of the implemented ECG system.

Parameter	Value	
Power	10	W
MPP Voltage	16.8	V
MPP Current	0.59	A
Short-Circuit Current	0.65	A
Open-Circuit Voltage	21	V

Table 1: BP Solar module characteristics.

Trial	Output Power w/o reconfiguration [W]	Output Power with reconfiguration [W]	Power enhancement [%]
#1	47.47	49.62	5
#2	19.07	44.27	132
#3	14.34	24.82	73
#4	14.89	24.21	63
#5	12.25	13.38	9
#6	20.45	43.70	114
#7	22.23	42.27	90

Table 2: Power output under shaded and unshaded conditions.

An All-Digital Spike-based Ultra-Low-Power IR-UWB Dynamic Average Threshold Crossing Scheme for Muscle Force Wireless Transmission

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In this work an Impulse Radio Ultra-Wide Band (IR-UWB) transmission scheme for miniaturized biomedical applications [1], based on a dynamic and adaptive voltage thresholding for surface Electro Myo Graphy (sEMG) signals and referred to as Dynamic Average Threshold Crossing, D-ATC, is proposed. The input to the proposed D-ATC is an amplified sEMG signal which is compared with a voltage threshold generated by a DAC (Set_Vth) to dynamically control the "firing rate" of the IR-UWB transmitter. The output of the D-ATC is in turn D_in, synchronized with the D-ATC system clock, to be processed by the next modulator [2]. The 4-bit DAC used in this work creates a voltage threshold (Vth) that varies from 0 to 1V with 16 steps, accurate enough for this application. The D-ATC uses the one bit signal D_in to examine the mean time when sEMG signal is higher than Vth. For this purpose, at each clock cycle the counter in the D-ATC architecture (Fig. 1) is increased when D_in='1'. The block adjusts the Vth level by monitoring the number of ones and zeros of D_in during a frame. The frame length is programmable (Frame_selector signal) and can be 100, 200, 400 or 800 times the system clock period. In order to have an adaptive voltage threshold, it is required to implement a feedback from the previous frames data. Trading-off complexity and accuracy, three last frames are selected to count the number of ones (referred to as N_one_i). Thus, weighted average of the number of ones in the last three frames is computed by using the following weights: WF3 = 1,WF2 = 0.65,WF1 = 0.35, obtained through real experiments. Simulation results compare D-ATC with a fixed threshold Average Threshold Crossing (ATC) system [3] demonstrating improved robustness (see Fig. 2, left part). The proposed thresholding algorithm has been verified on a dataset of 190 sEMG recorded signals. The resulting events and the associated digitalized voltage level can be both asynchronously radiated through an IR-UWB transmitter [2]. Analysis of the results, shown in the right part of Fig. 2, highlights that the scheme is robust w.r.t. the sEMG signal variability and correlates by ~96% with regard to raw muscle force information after signal is recomputed at the RX. The proposed D-ATC digital control logic has been implemented and simulated on a 0.18μm CMOS process, showing reduced power consumption (about 70 nW of dynamic power consumption) at very low active area expenses (about 11700 μm^2). Recently we received the chips in a CPGA208 package, thus a PCB to test the chip in a real environment is currently under development.

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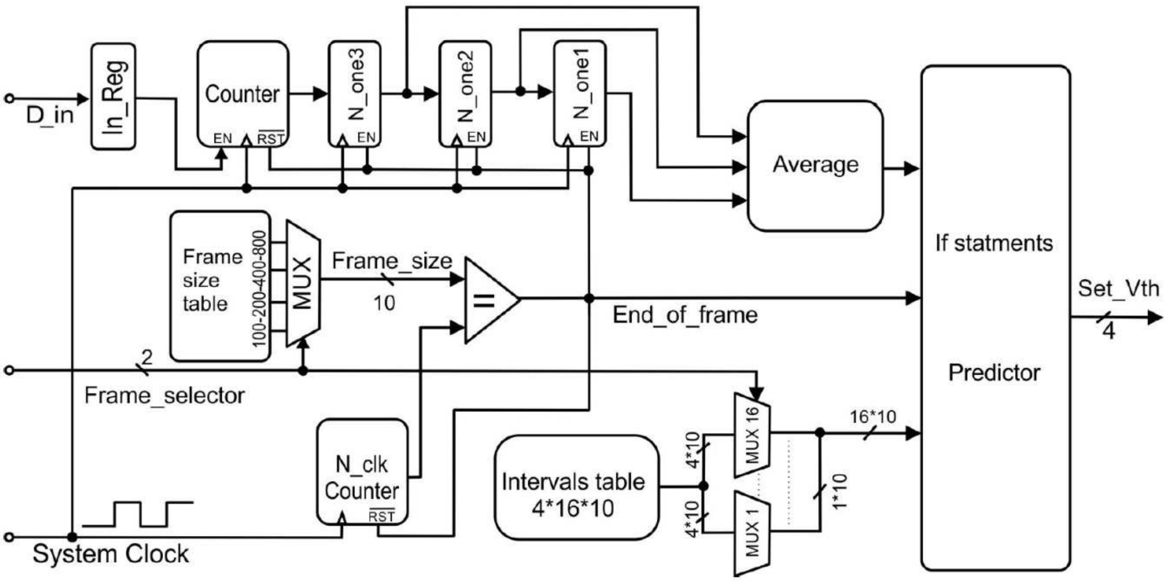

Figure 1 D-ATC controller architecture.

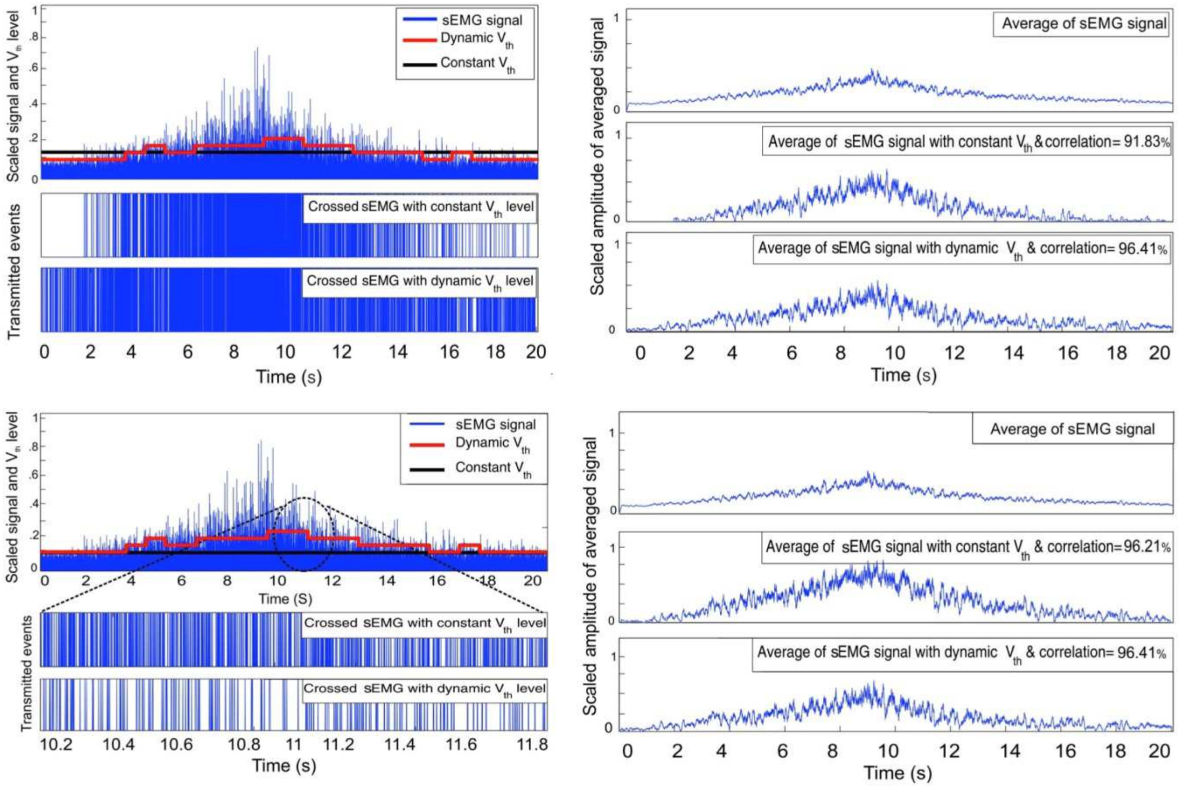

Figure 2 ATC and D-ATC comparison.

An embedded platform for volatile chemical localization and mapping with *any* mobile carrier

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Unmanned Aerial Vehicles or *drones* are nowadays very popular and widely used in scientific research for distributed data collection and remote sensing [1], particularly because of their advantages, like precise positioning and high resolution imaging, which are essential in environmental science and engineering related studies [2]. Moreover, drones can be easily driven in remote locations and harmful environments, while safeguarding the health of operators, to fulfill dangerous tasks. At the same time, increasingly strict regulations on air quality and environmental pollution, require new instruments for people to assess the safety of industrial and public spaces.

In this work, we present an embedded electronic platform (Figure 1) able to instrument any kind of drone with a chemical sensing system for environmental monitoring, gas leakage detection and pollution mapping applications. We developed a lightweight electronic system, based on a 32MHz/32bit wireless microcontroller unit that manages a GSM/GPS modem, a digitally controlled analog interface to drive MOX gas sensors and a micro Sd-card for local logging. The two wireless interfaces, a short range 2.4GHz radio based on the IEEE 802.15.4 standard and the GSM/GPRS one, allow the development of custom and smart applications for real-time data sharing and/or alarm notification. The complete 16 cm^2 board (4x4 cm) is battery powered (Li-ion 1800mAh) and the total weight is less than 30gr. The remarkably low weight allows the choice of any kind of carrier, not only UAVs, but also wheeled robots, public transportation means and so on.

The most important design parameter is the energy autonomy of the drones for gas leakage localization and mapping which deals with weight of the system (the payload) and electrical power consumption. No commercial drones exists with autonomy longer than one hour and MOX gas sensors, like GSM modems, consume a remarkably amount of power. For this reason we conducted a set of simulations to evaluate the optimal tradeoff between speed of the carrier, energy consumption and gas localization capability.

Starting with the characterization of the prototype in terms of energy consumption (Table 1) and time requirements for each task (Table 2), we selected a target application scenario and developed an optimal monitoring algorithm to run the simulations. We used a 2D model of the environment and linear motion equations for the drone, which abstracts a pipeline monitoring task with a unique gas leakage source (modeled with a Gaussian distribution function). We developed a hill-climbing based algorithm to drive the autonomous drone search (flowchart of the algorithm is presented in Figure 2), which working principle is depicted in Figure 3.

Simulated results (Figure 4), evaluated as energy consumption with respect to distance of the leakage and starting speed of the drone, show how to evaluate the optimal starting speed which reduces the total energy consumption and potentially allows for a wider monitoring areas.

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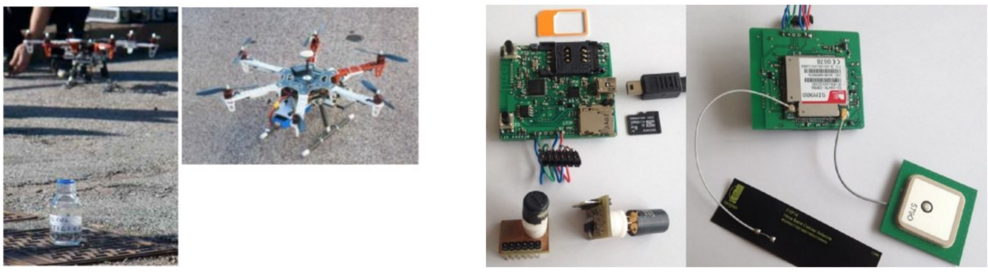

Figure 1. The prototype embedded sensing system.

Table 1. Average consumption of the prototype measured using 1Ω shunt resistor.

Status			Consumption
MCU	GPS/GSM	MOX	[mA]
sleep	off	off	<1
on	off	off	12.50
on	off	on	51.25
on	on	off	33.75
on	on	on	75.00
on (LogSD)	off	off	35.60
on (LogSD)	on	off	56.25

Table 2. Time requirements of single tasks.

Task	Time [ms]
LogSD	150
ADC Measure	1026
GPS request	5125
Mean Measure	5
Total	**6805**

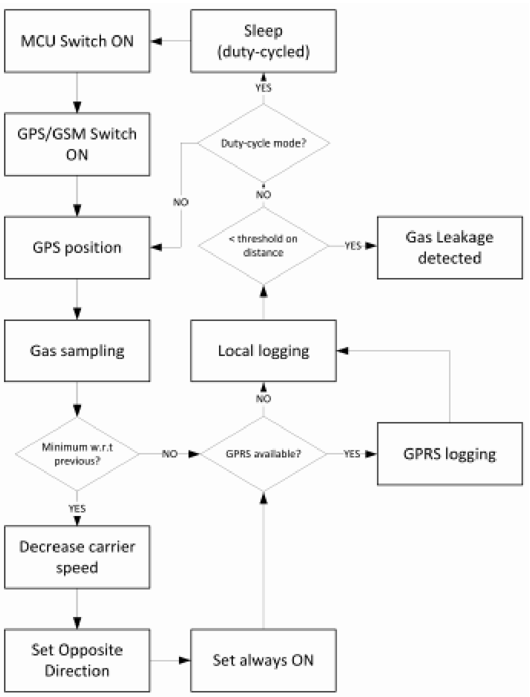

Figure 2. Tracking algorithm flowchart.

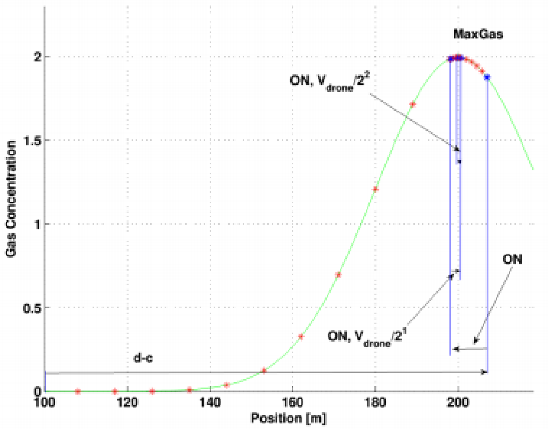

Figure 3. Tracking algorithm example.

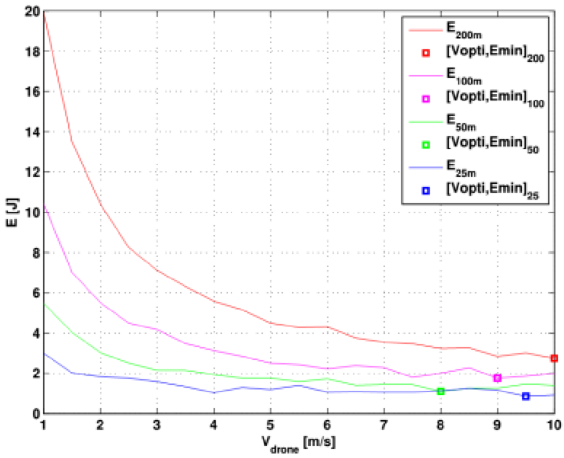

Figure 4. Tracking algorithm optimal starting speed w.r.t leakage distance.

Design of an electronic conditioning system for the multi-sensor detection of charged moving debris

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In this work we investigated a solution for the design and the implementation of an electronic conditioning device to be used in a multi-sensor detection system for charged moving debris. The electrostatic detection of charged debris has been proposed in literature as a tool for the condition monitoring of industrial gas turbines. A typical debris detection system is based on electrostatic sensors and charge amplifiers.

On the basis of the study presented in [1] in turbo-machinery applications the charge signal frequency spectrum is typically distributed in the low-frequency range, and a particular care has to be placed in the design of the charge amplifier frequency response. Accordingly, we proposed an improved charge amplifier operating with different programmable nominal gains (0.01V/pC, 0.1V/pC, 1V/pC, and 10V/pC) and different programmable bandwidths (high-pass cut-off frequencies 0.1Hz, 1Hz and 10Hz).

The design of the charge amplifier was based on a circuit model proposed in [2] and reported in Fig.1 for which we provided a detailed circuit analysis involving analytic calculations and numerical simulations to meet the design specifications. On the basis of the obtained results, a proper selection of the circuit off the shelf components has been performed for the physical realization of the device.

In order to set different operative design specifications of the charge amplifier we implemented a serial communication protocol supervised by an Atmel microcontroller embedded in the board and programmed with the Arduino design environment.

We have characterized the implemented device in terms of frequency response in the frequency range 0.1 Hz - 1MHz. To this end, we developed an automated measurement system using the LabVIEW design environment. This software provides the possibility to program the different functions of the charge amplifier and to control the measurement instrumentation by a PC.

According to the design specifications, the instrument high-pass cut-off frequencies determined by the first stage of the implemented device (i.e., the input charge amplifier) are properly obtained at the frequencies 0.1Hz, 1Hz and 10Hz. Also the overall gain in the pass-band is in accordance with the design target values, with a moderate deviation (less than 4%) with respect to the design goals.

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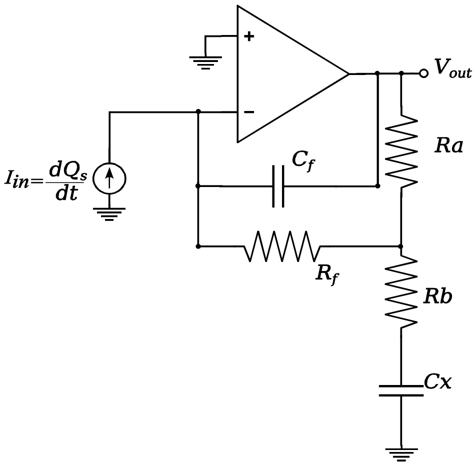

Figure 1: The charge amplifier circuit used to design the first stage of the electronic conditioning system.

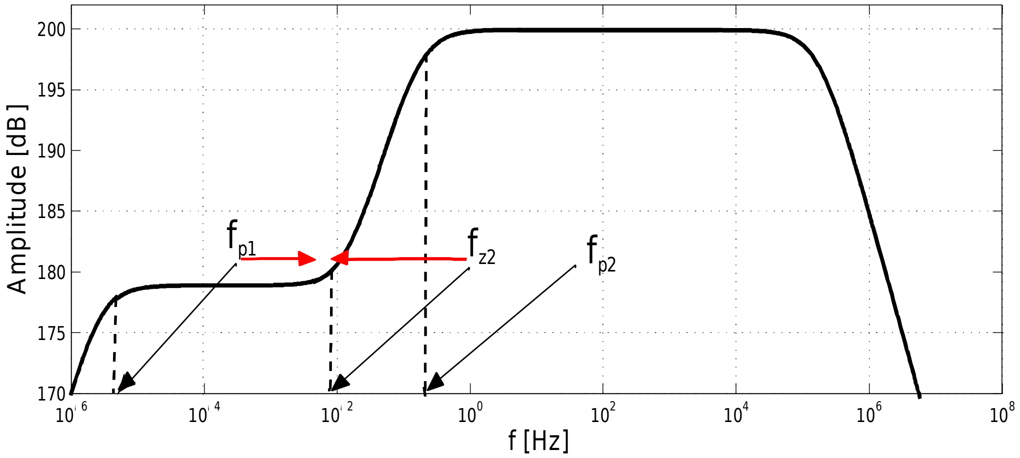

Figure 2: Frequency response design and analysis.

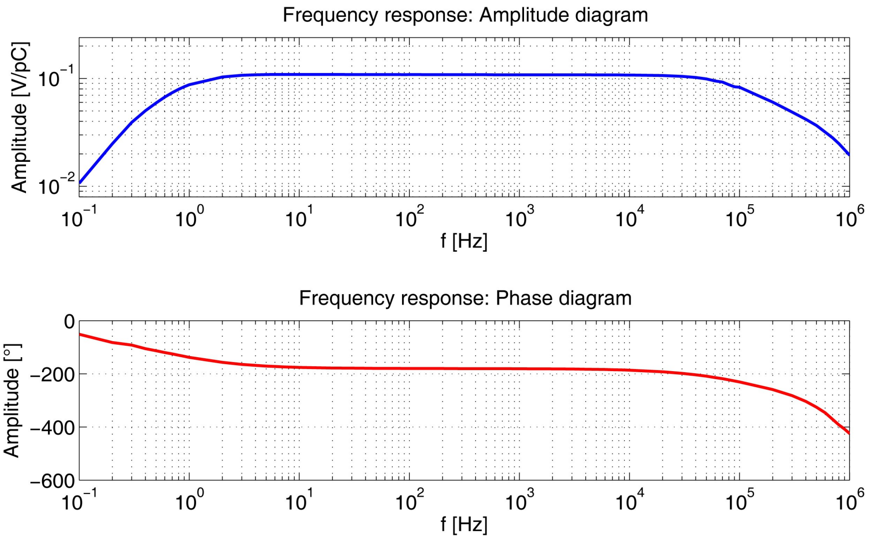

Figure 3: Measured device frequency response ($G = 0.1\text{V/pC}, f_{p2} = 1\text{Hz}$).

Dual Band Architecture For High Conversion Efficiency Energy Harvesting System

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Nowadays energy recovery from environmental power sources is an innovative and appealing way to capture and store energy for small, wireless and autonomous devices commonly used in wearable electronics and wireless sensor network systems [1]. In the last years, the number of ”free” energy feeders is rapidly increasing thanks to the new broadcast TV channels and the wide diffusion of WiFi hot spots and mobile telephone repeaters. On the contrary, the EM energy radiated by feeders is difficult to catch, since it is time-dependent and heavily related to the number of users and the surroundings. The proposed contribution shows an innovative system for energy harvesting, based on a dual band architecture and able to handle both GSM and WiFi signals. A typical scenario for the fabricated prototype board is shown in Figure 1. The key points of the designed circuit are the capability to manage input signals over a wide power range together with the high energy conversion efficiency in the full band. The power handling characteristic is an important feature for energy harvesters since they are usually located in unknown environments with time-variable and random signals of unknown energy [2-3]. In addition, conceiving the proposed architecture as suitable to be used in urban environment, the dual-channel receiver has been tuned at 936MHz and 2.4GHz, so to catch the largest amount of EM radiation in the surroundings. In Figure 2, a block diagram of the system is shown. It has a dual-channel structure, each of which designed to manage different power levels at both the reference frequencies. The power control unit can switch the incoming signal to the proper AC/DC converter through a feedback control and comparing the input power to the reference power threshold of each channel. In this way the dynamic range of the full system comes from -20dBm to 20dBm for both the frequency bands. The power-variable incoming signal is rectified into a DC component and then managed by the storage and regulation section that allows to transfer the DC voltage source to the load, as, for instance, a researchable battery or an end user.

The main goal of the proposed design has been to ensure a high transducer gain for the incoming EM signals. Defining the harvester efficiency as the ratio between the rectified power and the input one, the proposed circuit shows an efficiency greater than 60% for an incoming power between 5dBm and 15dBm and it decreases to 40% in the power range between -10 dBm and 20dBm, thanks to a suitable design of the matching networks and of the control system. The simulated results about efficiency are shown in Figure 3. Test measurements of the proposed system have also been performed with similar results.

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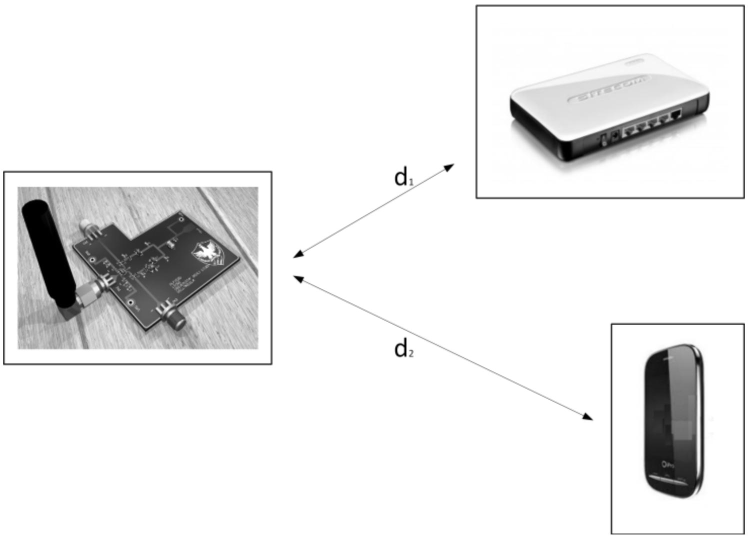

Figure 1: Experimental setup: prototype versus mobile phone andWi-Fi router.

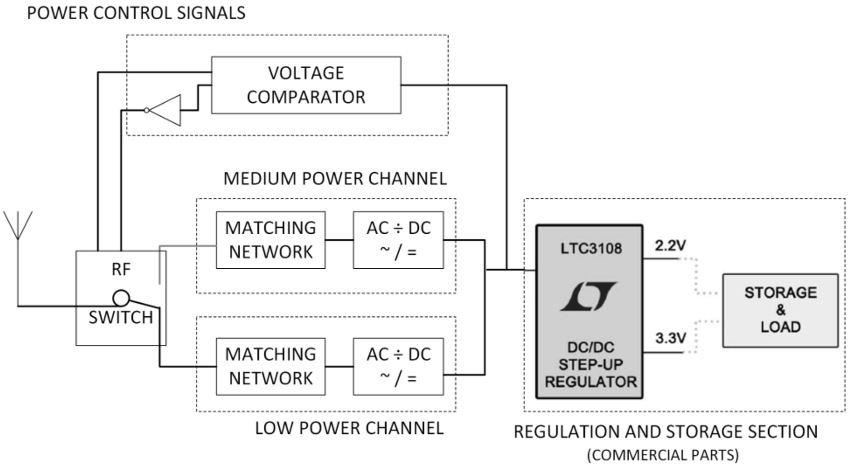

Figure 2: Proposed dual band harvester block diagram.

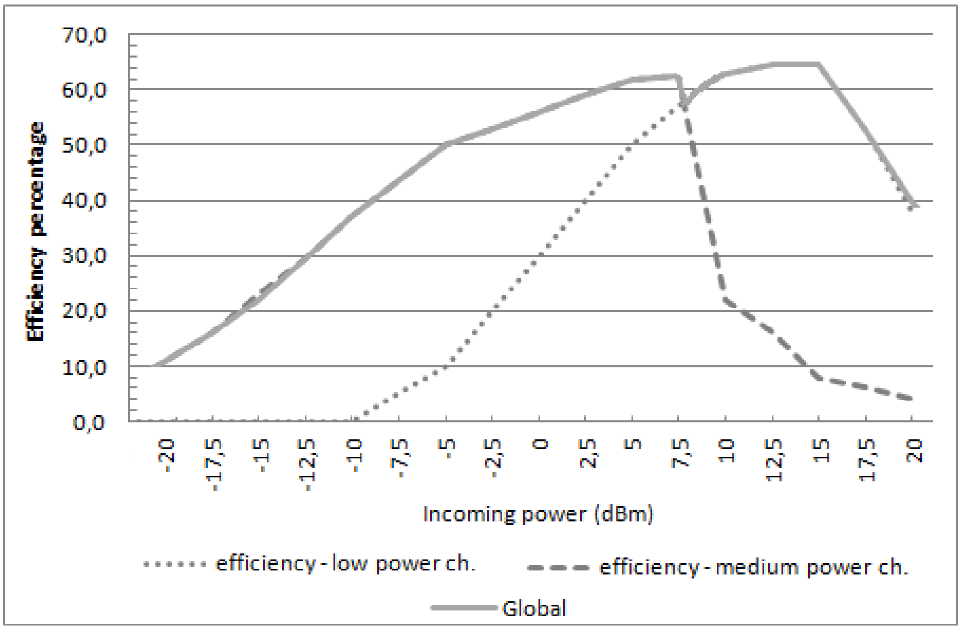

Figure 3: Double input efficiency – test results

Efficient Implementation of H.265 video decoder on low computational power architecture

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Several compression standards have been developed in the past years, among them H.264/AVC is the most recent video coding standard [1]. HEVC/H.265 aim is to increase the compression efficiency by 50% if compared to the H.264/AVC, while maintaining the same level of visual quality. In Fig 1, the HEVC decoder block diagram is illustrated. The main difference with previous standard is the flexible picture partitioning. In this paper, we will focus on an optimized software implementation of the HEVC/H.265 decoder, mainly exploiting data-level parallelism. In the description of the proposed approach, special regards is dedicated to the new H.265 features, highlighting the issues in exploiting data-level parallelism and proposing our solutions. Starting from results on performance achieved with test performed in our previous work [2][3], we have focused the optimization on the most computation demand modules of H.265. Our approach in previous software development was to use the Single-Instruction-Multiple-Data (SIMD) instructions to exploit the data level parallelism during the execution. We have improved SIMD optimization with a more efficient memory handling. In Deblocking Filter module, code reorganization has been performed in order to efficiently group load/store operations at the beginning/end of each vertical and horizontal phase. We have decided to write assembler code for prefetch and aligned load because we needed more flexibility respect to the NEON extension. In SAO Filter section we have exploited prefetch and aligned load/store like previously shown for debloking filter. The motion compensation (MC) has the purpose to create the temporal predictor that will be added to the decoded prediction error for creating the reconstructed block. We did a deep function specialization in order to separate luma from chroma motion compensation, monodirectional from bidirectional prediction, and no interpolation, only horizontal interpolation, only vertical interpolation or diagonal one. This process results in having 24 different functions specialized for each case. In order to evaluate the achieved performance after the optimization process, several tests have been performed on a set of test sequences, addressing 720p resolution and different coding features. Some of the results are shown in Table 1. The utilized architecture is the ARM Cortex A9 @1.2GHz with NEON extension. In Table 1, the decoding performance for a set of standard sequences is shown. The execution time is strongly influenced by the input stream configuration, but the optimized code is able to streams at 30 frames per seconds (fps). The random-access configuration shows the lower results, whereas using low-delay with only P slices lead to better performance. In the same table, we compare our results to the performance obtained with the reference decoder of the Joint Collaborative Team on Video Coding (JCT-VC), in order to put the here presented work in perspective. In particular, we refer to the H.265 decoder from the official software repository [4]. In the last three columns of the tables, we show the speed-up of our optimized decoder vs. the JCT-VC decoder. As can be noticed, the achieved performance are increased respect to our previous work.

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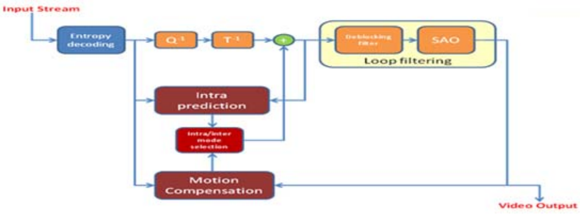

Fig 1. HEVC decoder block diagram

TABLE 1 – DECODER PERFORMANCE ON STANDARD SEQUENCES

Sequences	Number of frames	QP	Optimized decoder [fps]			JCT-VC decoder [fps]			Speed-up		
			LB	LP	RA	LB	LP	RA	LB	LP	RA
FourPeople	600	22	30.06	35.31	27.49	4.71	4.94	4.41	6.38	7.15	6.23
		27	38.43	49.01	31.96	5.86	6.16	5.05	6.56	7.96	6.33
		32	44.34	57.44	35.49	6.63	6.87	5.39	6.69	8.36	6.58
		37	50.09	65.06	38.10	7.34	7.45	5.70	6.82	8.73	6.68
Johnny	600	22	29.80	36.33	28.96	4.69	5.01	4.37	6.35	7.25	6.63
		27	39.10	52.14	36.65	5.82	6.41	5.12	6.72	8.13	7.16
		32	45.13	60.21	39.26	6.54	7.07	5.45	6.90	8.52	7.20
		37	49.86	66.86	42.25	7.28	7.55	5.74	6.85	8.86	7.36
KristenAndSara	600	22	27.17	32.88	26.12	4.16	4.58	4.00	6.53	7.18	6.53
		27	34.52	43.69	31.75	5.02	5.56	4.57	6.88	7.86	6.95
		32	40.46	51.96	35.47	5.69	6.20	4.94	7.11	8.38	7.18
		37	45.70	58.36	38.64	6.39	6.74	5.29	7.15	8.66	7.30
SlideEditing	300	22	48.21	64.23	39.93	8.38	8.31	5.98	5.75	7.73	6.68
		27	51.61	67.43	40.56	8.48	8.40	6.01	6.09	8.03	6.75
		32	52.56	71.62	38.77	8.54	8.45	5.96	6.15	8.48	6.50
		37	55.08	73.67	39.35	8.71	8.61	6.05	6.32	8.56	6.50
SlideShow	500	22	37.02	45.42	31.25	5.90	5.96	4.90	6.27	7.62	6.38
		27	40.83	50.40	33.38	6.19	6.22	5.08	6.60	8.10	6.57
		32	46.22	56.51	34.96	6.48	6.53	5.25	7.13	8.65	6.66
		37	49.12	60.55	37.02	6.80	6.83	5.36	7.22	8.86	6.91

Nano-power ICs for Energy Harvesting Applications in the Internet-of-Things

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As electronic technologies progress, a growing number of miniaturized smart devices is populating the Internet of Things (IoT) and paving the way towards the Abundance of connected sensor nodes [1]. Environmental energy harvesting is a promising technique to explore, although still far from being mature, as power budgets are not satisfied in most envisioned applications since state-of-the-art power converters still require several µW to function. This abstract reviews a series of power conversion ICs for energy harvesting applications down to 1 µW input power, and comments on their use in a series of applications.

The first design targets power extraction from small-sized piezoelectric transducers [2]. The circuit (Fig. 1a) implements Synchronous Electric Charge Extraction (SECE) with the novel addition of Residual Charge Extraction (RCI) for boosting performance at low input voltages. A two-way energy storage policy is implemented for granting very fast start-up times even in presence of ultra-large storage capacitors. The IC draws a quiescent current of 160 nA and achieves a 85% energy conversion efficiency. The second design is a fully autonomous power converter for energy harvesting from multiple and multi-type sources such as piezoelectric, photovoltaic, thermoelectric and RF transducers [3]. The circuit (Fig. 1b) adopts a single time-shared inductor operating in discontinuous current conduction mode. The intrinsic power consumption of the circuit is as low as 48 nA/source, with energy conversion efficiencies up to 89.6%. Both ICs are designed for full battery-less start-up and operation.

From an application point of view, low intrinsic power consumptions allow positive power budgets even in harsh power conditions, where present state-of-the-art circuits fail to operate, so that smart nodes can be deployed pervasively with no wires or batteries. In a first set of applications, a wireless temperature sensor node (Fig. 2) and a wireless fall detection system (Fig. 3) were developed using ultra-low power MCUs and micropower sensors. System optimization allowed consuming respectively less than 400 µJ and 150 µJ per each cycle of operation (node wake-up, sensing, wireless transmission). Besides, the use of the above IC in multi-sensor wireless sensor nodes [4] is currently being investigated in collaboration with industrial partners. A draft rendering is shown in Fig. 4, where the multi-source energy harvesting IC manages piezoelectric, PV, and thermoelectric transducers for supplying a multi-sensor wireless platform achieving a positive budget for a system including a low-power accelerometer, temperature and pressure sensors, and a BlueTooth Low Energy (BTLE) wireless interface for standard communication with next generation mobile devices.

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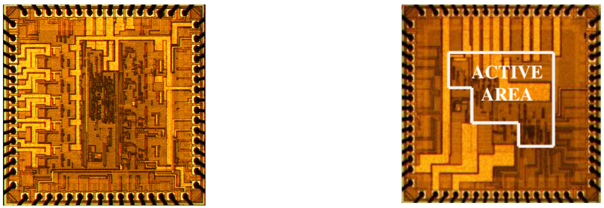

(a) (b)

Figure 1: (a) A multisource energy harvesting IC [3] from multiple heterogeneous types of sources; (b) a piezoelectric energy harvesting IC [2] with residual charge inversion and two-way energy storage. Both ICs were implemented in a STMicroelectronics 0.32 µm process in a die area of 4.6 mm^2.

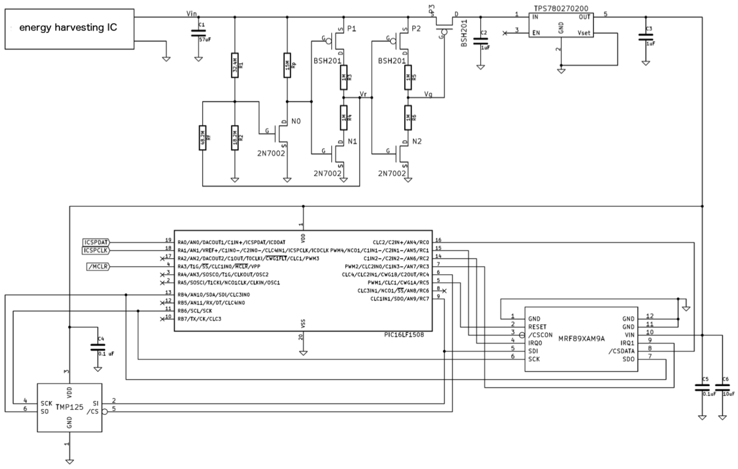

Figure 2: A battery-less and energy autonomous micro-power wireless temperature sensor node.

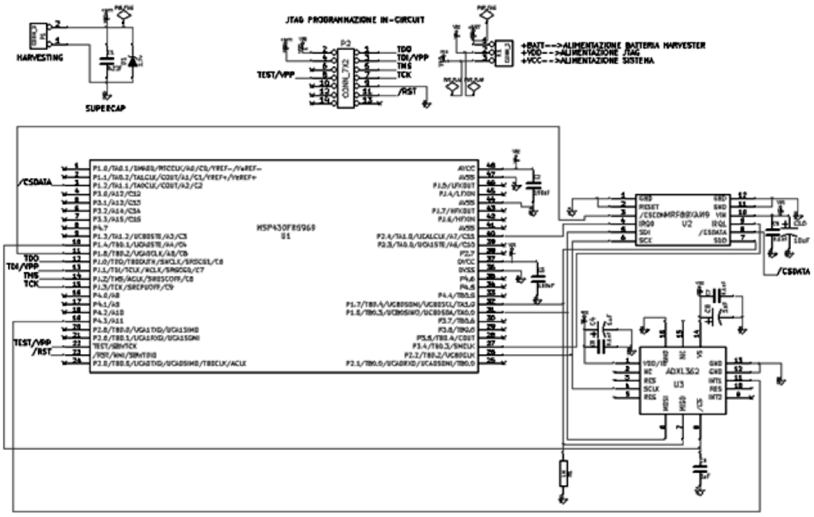

Figure 3: A battery-less and energy autonomous wireless fall detection and alert system.

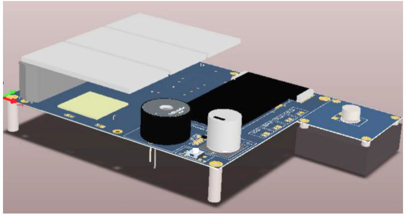

Figure 4: A sketch of the power management module currently under development and based on the IC shown in Fig. 1a for a wireless multi-sensor platform including a low-power accelerometer, temperature and pressure sensors, and a BlueTooth Low Energy (BTLE) wireless interface.

OpenSpatial ready µ-sized, high-performance AHRS module for the Internet of Things era

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In the next years wearable devices will far overtake every market expectations, becoming the fastest ramping consumer technology device up to date, even more than smartphones and tablets [1]. Millions of devices will be connected together, providing remote management of everyday things and detection of a wide number of biometric parameters.

Inertial Measurements Units (IMUs) provide the core functions for any wearable and embedded device essentially, and are the most promising technologies in applications where an accurate and reliable estimation of limbs position and orientation is required. These systems, typically based on the combination of a triaxial geomagnetic sensor (MARG: Magnetic, Angular Rate, Gravity) and a microcontroller, can be enhanced by means of a Bluetooth radio interface. The orientation estimation processing can be performed on board, leading to an Attitude and Heading Reference System.

This work presents a downscaled, high performance and low energy AHRS module particularly attractive to capture gestures with a low-latency (less than 10 ms) and fast response time, devised for rehabilitation, industrial and sport applications, as well as for gaming in consumer electronics.

Thanks to the recent improvements in reducing power consumption in electronic devices, a miniaturized and wireless multi sensing platform has been designed. The G-Module platform is a surface-mount PCB module that provides a fully embedded and ready to use wireless AHRS. Fig. 1 shows the block diagram, Fig. 2 the developed module and Fig. 3 depicts the schematics of the platform. The G-Module is based on the STM32F411MCU operating at 16 MHz, a 3D accelerometer, a 3D gyroscope and a 3D magnetometer. The availability of 9 DOF makes it possible to estimate the 3D orientation and position of the platform, enabling the system for gesture recognition. All these features are compliant with the OpenSpatial specifications, a set of standard service profiles [3] for Bluetooth V4 radio interface. It has been mostly designed to foster innovation of new hardware without changing the software interface with the wearable device (e.g. mobile application). Service profiles include characteristics for the transmission of position in the space, the orientation, the recognized gesture, motions and button status.

Results

The presented platform is a µ-sized module in a 13.5 mm × 13.5 mm form factor with a low power consumption, suitable to be wearable. The small dimensions make it ideal for gesture recognition as well as sleep and physical activity monitoring or environmental parameters logging. G-Module could be used in several industrial fields such as transport monitoring and medical devices tracking for insurance purposes.

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[3] OpenSpatial specification, NOD-labs, official web-site: https://github.com/OpenSpatial/.

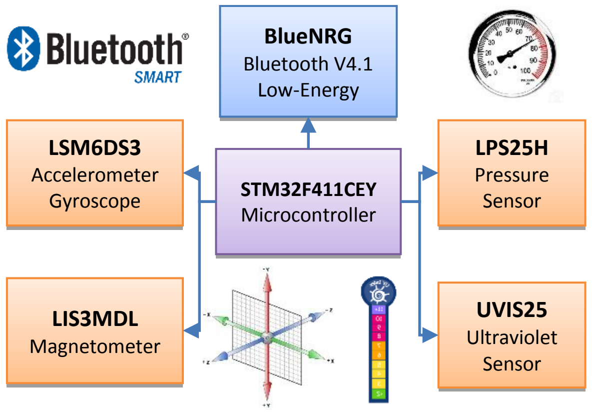

Figure1: G-Module block diagram. The BlueNRG Bluetooth chip and the sensors are connected to the MCU with the same SPI bus

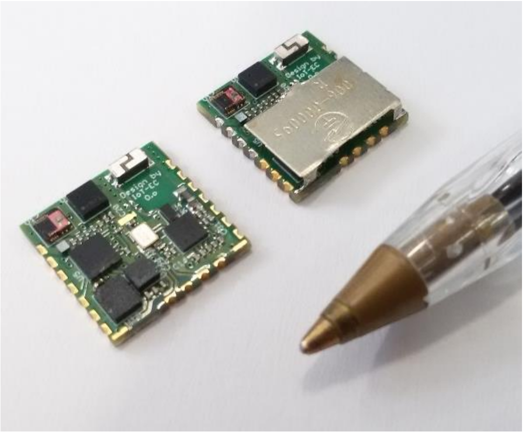

Figure2: G-Module without and with metallic shield in a 13.5 x 13.5 mm^2 form factor

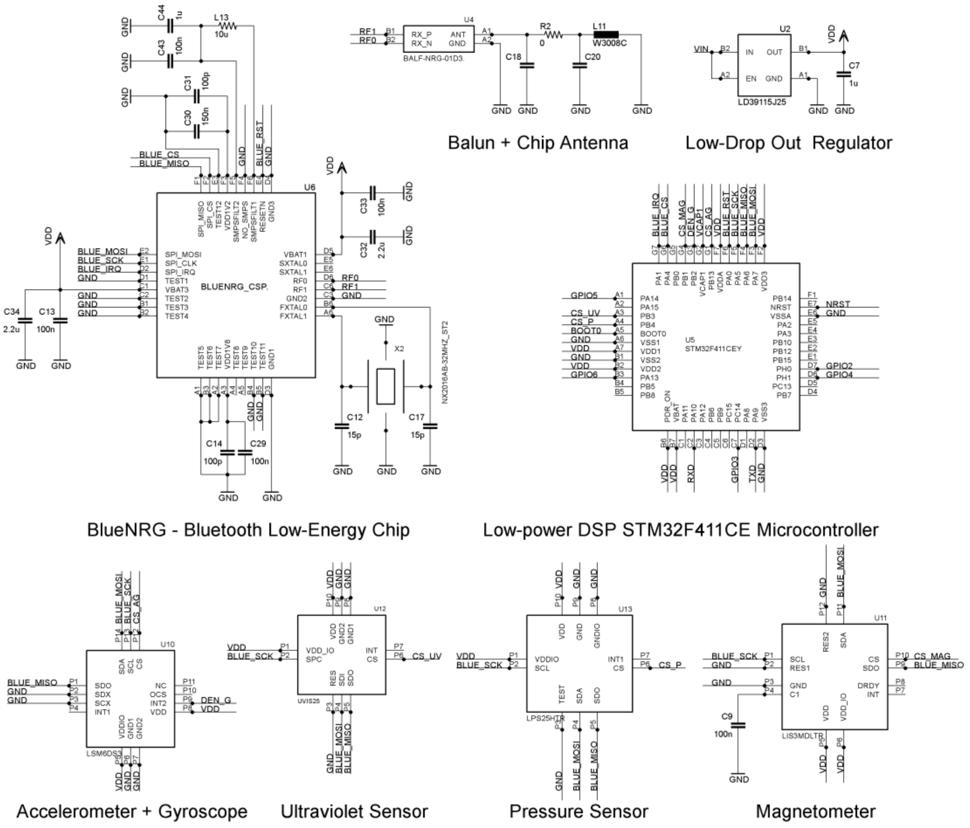

Figure 3: The G-Module schematics

Pilot tone as a key to improving the spatial resolution of eBPMs

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Beam Position Monitors (BPMs) are fundamental tools for particle accelerators: their task is to measure the position of the particle beam, allowing the orbit correction system to stabilize it. Typically, the position is obtained by using a difference-over-sum algorithm involving the signals coming from four electrodes mounted inside the chamber (in this case, the electrons storage ring) [1, 2].

At Elettra, the Italian synchrotron light source, an internal project has been started to develop an electron beam position monitor capable of achieving sub-micron resolution with a self-compensation feature. To fulfil these requirements, a novel RF front end has been designed.

A high isolation coupler combines the input signals with a known pilot tone which is generated by the readout system. This allows the parameters of the four channels to be continuously calibrated, by compensating the different responses of each channel. A similar technique is already known [3, 4], but for the first time experimental results have shown the improvement in resolution due to this method.

The RF chain was coupled with a 4-channel digitizer based on 160 MHz, 16 bits ADCs and an Altera Stratix FPGA. At first, no additional processing was done in the FPGA, collecting only the raw data from the ADCs. The position was calculated through the FFT of each signal.

A MATLAB simulation was also performed to verify the analytic relation between spatial resolution and signal-to-noise ratio; this was very useful to better understand the behavior of the system with different sources of noise (aperture jitter, thermal noise, etc.).

The experimental data (taken with an RF generator that emulates the signal of the beam) were compared with the simulation, showing a perfect agreement with the latter and confirming the capability of the system to reach sub-micrometric accuracy. Therefore, the use of the pilot tone greatly improves the quality of the system, correcting the drifts and increasing the spatial resolution by a factor of 4 in a time window of 24 hours.

Additionally, the whole system was connected to real transducers (pick-ups) in a section of the storage ring of Elettra: several data were collected, confirming the necessity of the compensation to get reliable measurements.

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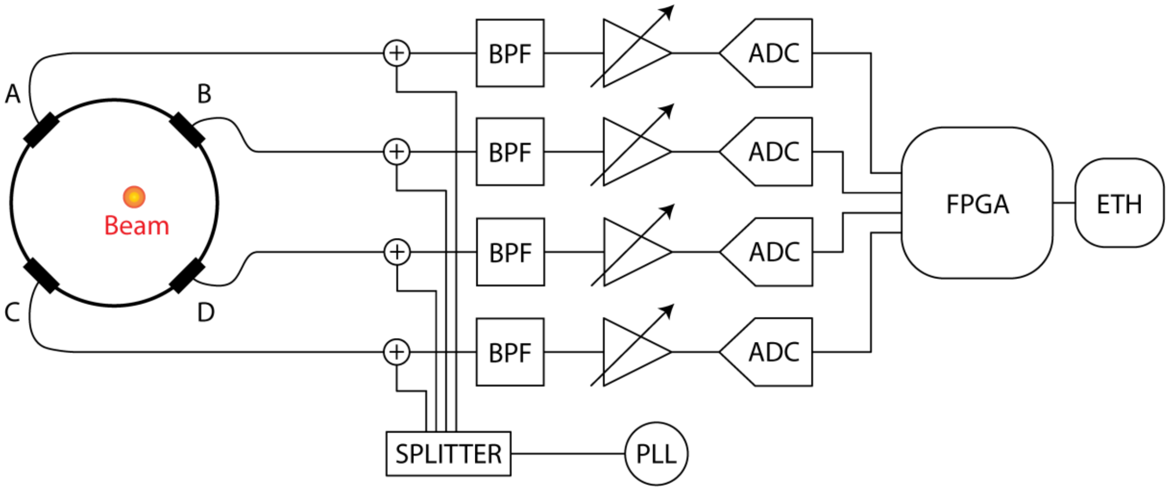

Figure 1: Block diagram of the system. From left to right: chamber with four electrodes, combiners, bandpass filters, variable gain amplifiers, analog-to-digital converters, FPGA with Ethernet connection. Below: PLL for pilot-tone generation.

Portable electronic system for a fast Radon indoor detection

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The World Health Organization (WHO) and the International Agency for Research on Cancer (IARC) have already classified radon as the second cause of lung cancer deaths. Radon (^{222}Rn) is a colourless, odourless, tasteless radioactive gas that comes from granitic or shale related areas in the ground. Indoor Radon detection can be used to assess the radioactive health risk in a given place [1-2]. The main disadvantage of the Radon detectors is that reliable concentration values are given after days or weeks. The main goal of this work is to develop a fast portable and small system with real-time indoor Radon detection capabilities, able to provide reliable Radon concentration in a few hours (approximately two).

The developed system, whose block diagram is depicted in Figure 1, with embedded processing and wireless communication capabilities, is based on a Zinc-Sulfat screen coupled to a Silicon Photomultiplier (SiPM) transducer, a low cost read-out electronics and a system ventilation. The device is able to monitor environmental data, so it could have multiple uses in research and industrial applications. The main goal of the readout Analog-Front-End is to collect, amplify and filter the charge signal produced by the SiPM, upon interaction with an alpha particle. The design of the air sampling system is strongly linked to the desired system resolution and measurement time. We designed a tubing system capable of moving such a flow (provided by an appropriate fan) to a measuring enclosed chamber (110x150x38 mm^3) with minimal losses, shown in Figure 2. Additionally to the electronic read-out components, the device includes an ultra-low-power 32 bit microcontroller. The processed data are transmitted via Bluetooth module to a mobile device, providing a real-time feedback to the user. In addition to Radon concentration, the module transmits each minute humidity and temperature values given by the environmental sensors, since the radon concentration and its decay products in dwellings show large temporal and local fluctuations due to the temperature, pressure, humidity, building material, ventilation condition, wind speed, etc [3].

Preliminary tests have been performed placing an alpha source (1nCi Am-241) on the active area of the ZnS scintillator, coupled with the SiPM. Figure 3 shows the alpha response of the third analog stage voltage output with 1 pixel and 16 pixels of the SiPM connected at the input. Further measurements were performed in order to analyse the correlation between the radon fluctuations and humidity, temperature and atmospheric pressure variations in the laboratory environment. The data obtained in the hourly record are shown in Figure 4. The averaged value of Radon concentration calculated during the acquisition is about 110 Bq/m^3, with a comparator threshold of 390 mV. The positive correlation coefficient (R = 0.4098) was obtained for atmospheric Radon concentration and humidity and for atmospheric pressure (R = 0.3311). Negative correlation values were calculated for temperature (R = - 0.44). The averaged radon activity values resulted to be higher than the mean value (90 Bq/m^3) measured by a commercial device (Corentium Canary). The reasons for this discrepancy could be attributed to various factors, such as detection algorithms, calibration and offset consideration, not only for the presented device but also for the commercial system (it gives reliable values only after several weeks). Further acquisitions are in progress in different conditions with the aim of finding the optimal system settings and fully validate the device.

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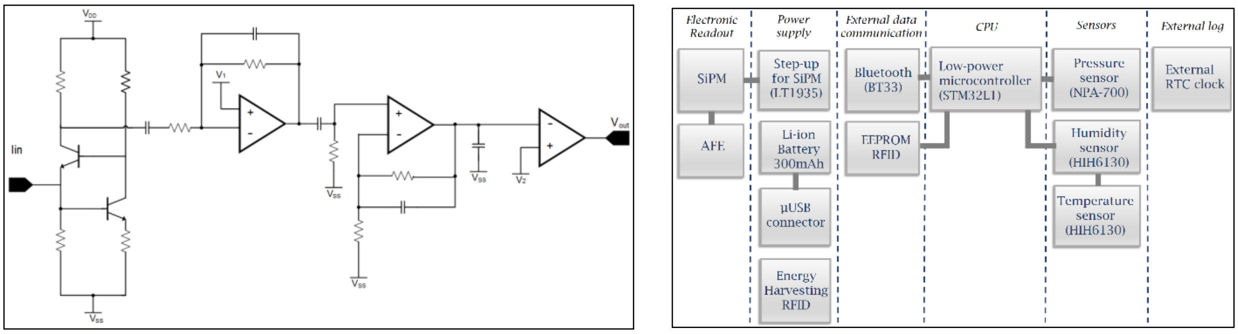

Figure 1: Analog-Front-End (left) and System block diagram (right).

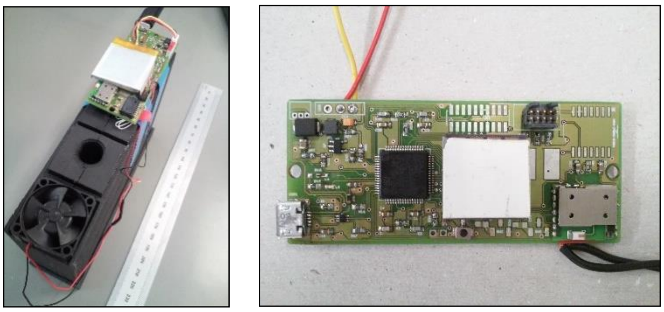

Figure 2: Tube ventilation coupled with the electronic platform (left) and the board assembled on a two layers 80x34 mm^2 standard FR4 PCB with commercial components (right).

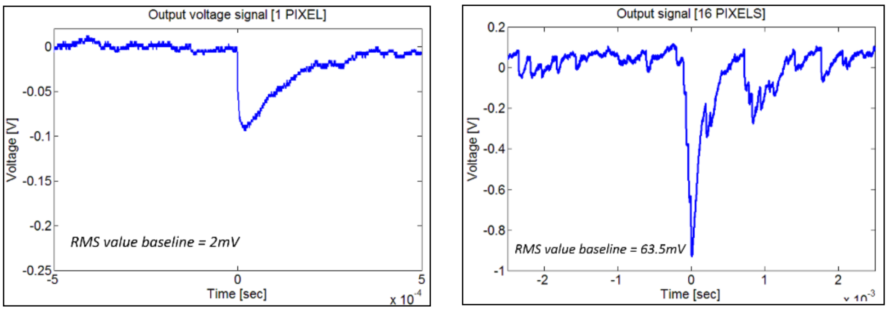

Figure 3: Output voltage signal with 1 pixel (left) and 16 pixel (right) connected.

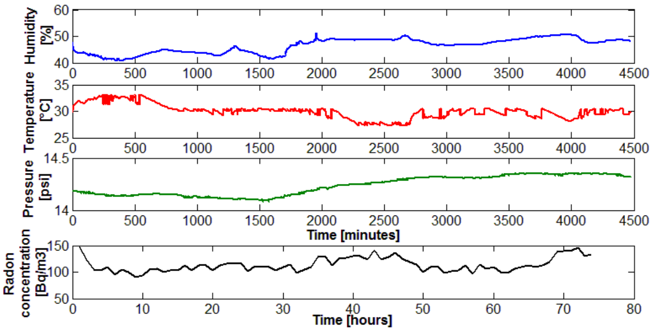

Figure 4: Environmental data and Radon concentration acquisition.

Reconfigurable Electronic System For Dynamic Radio Access

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The high number of wireless devices in the same environment usually leads toward a crowding occupation of the available channels. It causes channels saturation resulting in a decrease of the overall throughput. This is one of the main reasons why cognitive radio[1] and Software Defined Radio (SDR)[2] concepts were born. SDR is a promising radio technology that implements radio communication functionalities in software instead of hardwiring them within the silicon chips. Many current SDR platforms are based on General-Purpose Processor (GPP) architectures, such as PCs, but they need to deal with delay-related challenges, or on programmable hardware, such as Field Programmable Gate Arrays (FPGAs), hence leading to less simple programming step and longer development time. However to solve this problem a new programming environment, named Ziria[3], was developed; it includes a novel language and an optimizing compiler too. The hardware board, WARP v3 (Wireless open-Access Research Platform) shown in Fig. 1, is a scalable, extendable and programmable wireless community SDR platform, created at Rice University and integrating: a Xilinx Virtex-6 LX240T FPGA, two programmable RF interfaces and other suitable peripherals[4]. Moreover two MicroBlaze CPUs are implemented within FPGA. The high flexibility of this platform has been exploited to obtain a bandwidth reduction of the channel, for example to 5 MHz, useful for the introduction of new strategies for the channel adaptation and for more advanced sensing mechanisms. We extended the 802.11 Reference Design provided by the WARP team (Fig. 2), which natively supports the 20MHz channelization only. The available Virtex-6 FPGA resources were investigated: in particular clocking constraints of the Mixed-Mode Clock Manager (MMCM) and other custom core hardware IP Core (Intellectual Property Core). By customizing their behavior, the Wi-Fi channel bandwidth was changed from 20 to 5 MHz through two Xilinx tools: the Xilinx Platform Studio (XPS) and the Xilinx Software Development Kit (SDK). In particular an XPS generated bitstream and two software programs, one for each MicroBlaze, were implemented by using the SDK. The experimental test was carried out with two WARPs, one working as an Access Point (AP) and the second one as Station (STA). The successful association of the station has been checked at the layers 2 and above by the mean of PuTTY[5], while the spectral occupancy has been verified using an USRP[6] and the GNURadio software[7]. An example of the obtained 5 MHz channel bandwidth, at carrier frequency of 2427 MHz, is depicted in Figure 3.

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Figure 1: WARP platform

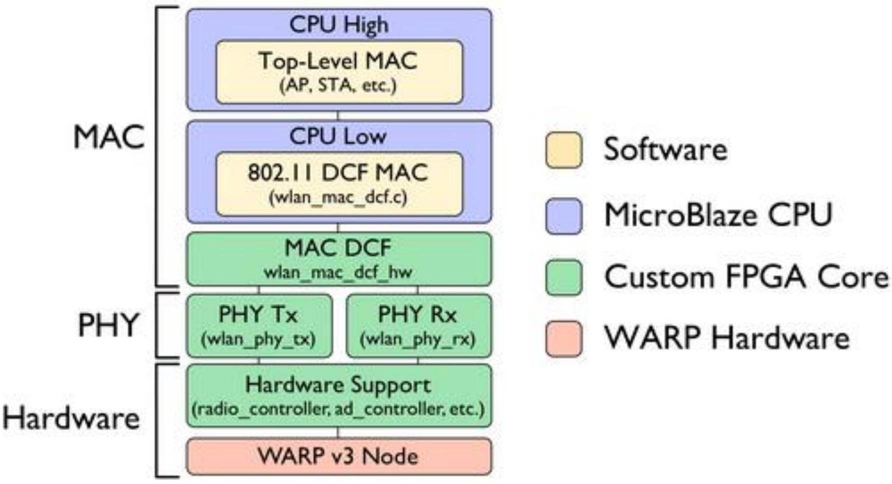
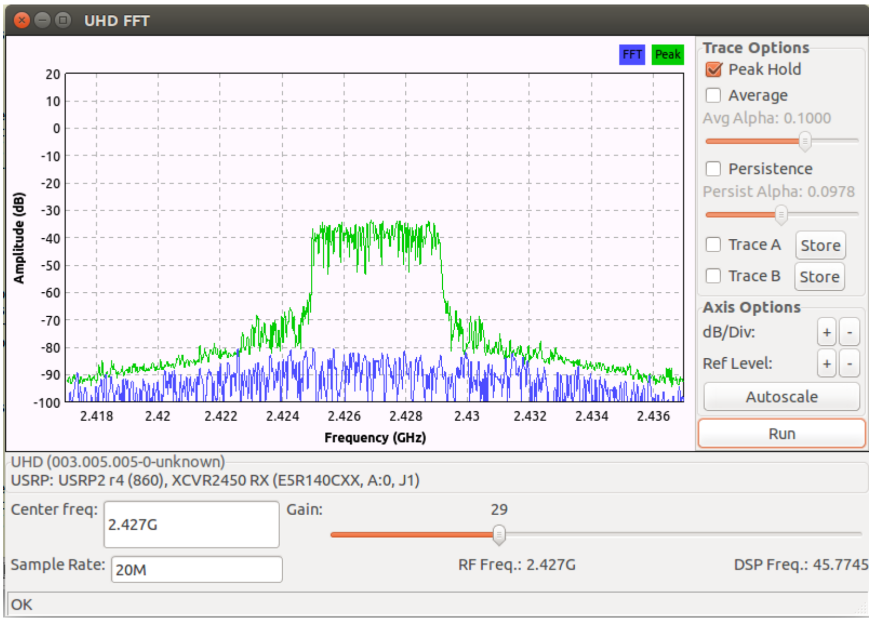


Figure 2: Reference Design 802.11 in the WARP platform



☑ Peak Hold
☐ Average
Avg Alpha: 0.1000
☐ Persistence
Persist Alpha: 0.0978
☐ Trace A
☐ Trace B

UHD (003.005.005-0-unknown)
USRP: USRP2 r4 (860), XCVR2450 RX (E5R140CXX, A:0, J1)

Center freq: 2.427G
Gain: 29
Sample Rate: 20M
RF Freq.: 2.427G
DSP Freq.: 45.7745

OK

Figure 3: FFT of the 5 MHz channel bandwidth test setup

RF Transceiver and FPGA-based Baseband Design of X-band Radars for Smart Mobility Systems

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Two FMCW (Frequency Modulated Continuous Wave) Radars operating in the X-band are presented for surveillance in smart mobility systems: monitoring railway crossing and ships in small harbors. The FMCW approach allows for detecting the presence of targets (e.g. obstacle on the railway crossing [1] or ships [2] in the harbor), as well as their speed and their motion direction. With respect to alternative solutions based on LASER, LIDAR or camera systems [3, 4] the Radar approach operates also in bad lighting and weather conditions, night and day.

For the harbor surveillance application the designed FMCW Radar transceiver has a center frequency around 10 GHz, a 300 MHz bandwidth swap, a repetition frequency of 1 kHz, a power amplifier of 2 Watts, a covered range up to 1200 m and a range resolution of 0.5 m. At receiver side multiple antennas (Fabry-Perot resonators with a 13 dBi gain) are used to estimate the direction of arrival along vertical and horizontal directions with a noise figure per channel below 5 dB and a 1dB input compression point of about – 30 dBm. The output of the X-band transceiver is then sampled at 12.5 MHz with a 14-bit ADC. Fig 1 shows the architecture of the Radar X-Band front-end developed in Microwave IC technology. The baseband signal processing, developed as a software running on a general-purpose processor by CNIT RASS [2], extracts range-speed maps of the targets and their shapes through interferometry algorithms. As an example, Fig. 2 shows the range-speed results of a test campaign held in a NATO contest at the harbor of the Italian Military Academy in Livorno. By using the same Radar without the final power amplifier stage the maximum transmitted power at the antenna is 1 mWatt and the covered range is up to 100 m.

For the railroad crossing safety application, developed in a partner collaboration supported by the Tuscany Region project SIMPLE with partners such as Italcertifer, IDS and INTECS, the radar front-end is operating around 9.5 GHz center frequency. The range resolution is up to 30 cm while the covered range is limited to few hundreds of meters, enough for the railway crossing. The whole data processing chain of the Radar system (Signal Processing Module) has been implemented on Xilinx Virtex-6 XC6VSX315T FPGA. The same FPGA also manages the low-level interfaces of the system with the external world (Control Module). The whole system, see Fig. 3, is organized as a network of 4 Radar nodes (Radar sensors in Fig. 3) placed at the 4 corners of the crossing and acting as clients plus a central server (Processing system in Fig. 3). The server node communicates with the national railway signaling system and is connected to a remote host in charge of railway traffic management. Each Radar node has a size of 60 cm x 30 cm x 20 cm and has been tested to reach a SIL 4 (Safety Integrity Level) thus being suitable for automatic control of railroad crossing.

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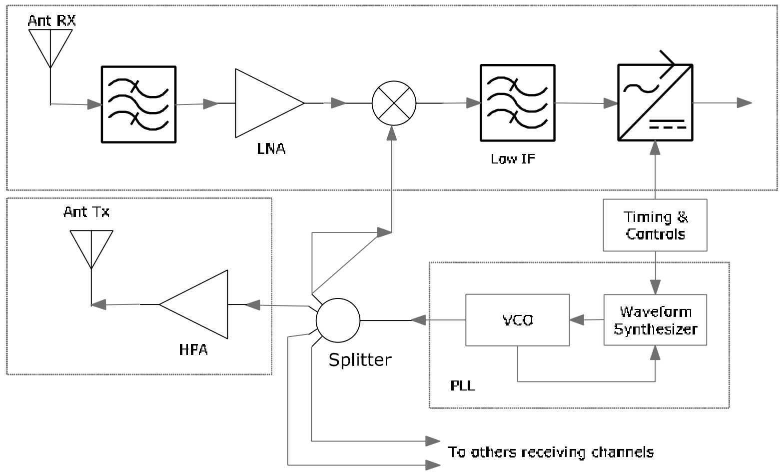

Figure 1: Architecture of X-band (10.55 to 10.85 GHz) front-end of the LFMCW Radar for harbor surveillance

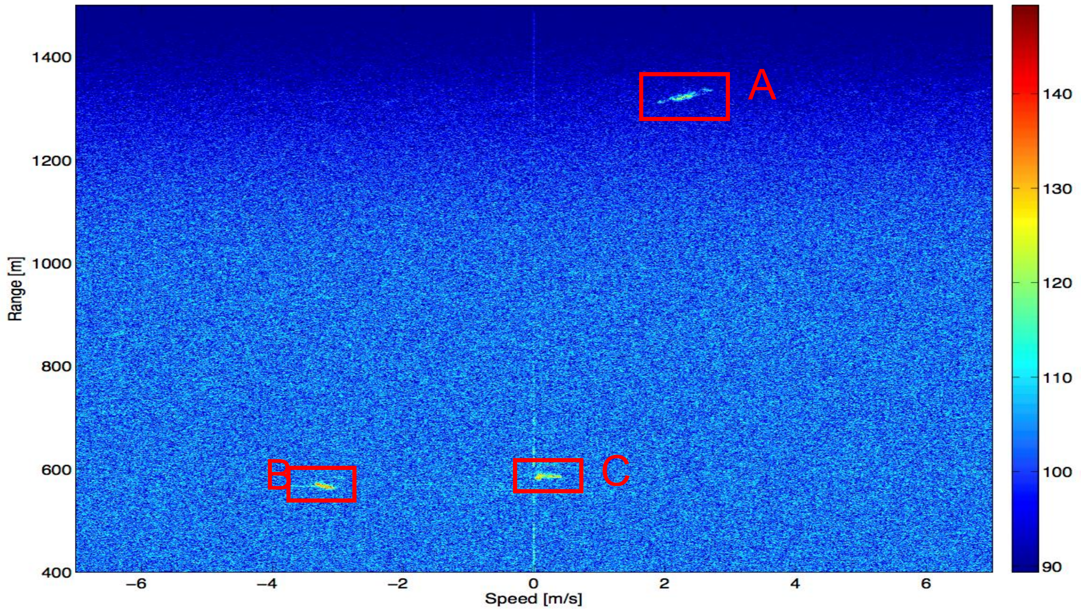

Figure 2: Range – speed map obtained with the X-band Radar of Fig. 1 during a NATO test campaign. 3 ships moving in the harbor of the Italian Naval Academy in Livorno, Italy

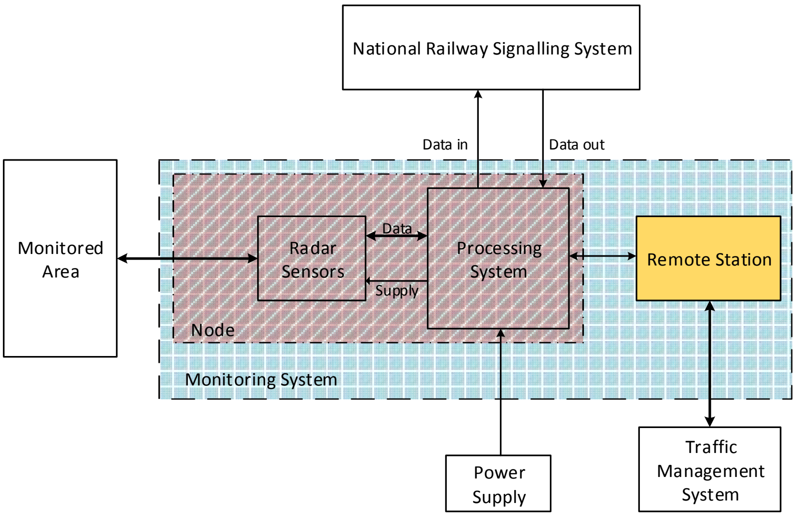

Figure 3: Radar sensing and processing nodes for railway/railroad crossing monitoring

Discussions with S. Lischi and R. Massini (CNIT RASS), P. Ruggiero and M. Righetto (IDS spa), R. Cassettari (University of Pisa) are gratefully acknowledged

Simple interference detection and classification in industrial WSN based on symbol error statistics

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Most of process control systems in use today are wired, showing a number of disadvantages, including costly commissioning and maintenance due to wrong cable installation and aging; reduced flexibility and data accessibility; and, last but not least, issues for ensuring intrinsic security. A viable option for monitoring purposes could be the adoption of (standardized) Wireless Sensor Networks (WSNs). Most of WSNs operate in the 2.4GHz ISM-band, the only license-free band available worldwide. Consequently, interference management is of utmost importance.

In this work authors propose and verify the performance of the Lightweight Packet Error Discriminator (LPED) algorithm, for detecting and classifying not only WLAN but also iWLAN interferences as well as multipath fading and attenuation (MFA). The iWLAN (where the ‘i’ stands for industrial) is a proprietary solution from Siemens derived from the IEEE802.11b/g purposely designed to satisfy high-throughput data transmission in large industrial areas. The core of iWLAN is the iPCF. Similarly to PCF, the traffic is handled according to a time division approach, where each station is provided with a 2-ms wide temporal window every cycle. However, differently from regular PCF function, iPCF does not include a contention period and a roaming protocol is also specified, allowing for switchover time on the order of 20-30 ms.

The LPED algorithm analyzes the symbol error density (SED, defined in Eq.(1), where c is the number of corrupted symbols in the packet, and sl and sf are the positions of the last and first corrupted symbol, respectively) in corrupted packets: Indeed, symbol errors caused by wireless communication systems tend to be grouped in a certain area of the packet, while errors caused by MFA are more randomly dispersed in the packet.

$$\mathrm{SED} = \frac{c}{s_l - s_f + 1} \tag{1}$$

Many measurements have empirically confirmed that usually SED≤0.2 for link under MFA, while WLAN and iWLAN interferers cause SED>0.2. The error location is determined using reed-solomon code, with a granularity related to the symbol length. Since WLAN bursts are usually shorter than 5bits and considering that typical packet size in industrial communication is small, the RS(15,7) code has been chosen. For testing the algorithm, a reference WSN operating in the 2.4GHz ISM-band has been implemented, composed of a Base Station (BS) regularly polling nodes who respond with a fixed size packet. The cycle time is TCYCLE=100ms and all the radios transmit using IEEE802.15.4-PHY at TXPOWER=0dBm. MFA derives from factory-like environments, while two scenarios with both WLAN and iWLAN have been considered as well.

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```
Decode the packet
if packet correctable then
    Calculate SED
    if SED≤0.2 then
        Packet is corrupted by MFA
    else if (0.2 < SED < 1) then
        Packet is corrupted by WLAN
    else if (SED == 1) then
        Packet is corrupted by MFA
    end if
else if packet uncorrectable then
    Estimate SED
    if (SED≤0:2) then
        Packet is corrupted by MFA
    else
        Packet is corrupted by WLAN
    end if
end if
```

Figure 1: The LPED algorithm.

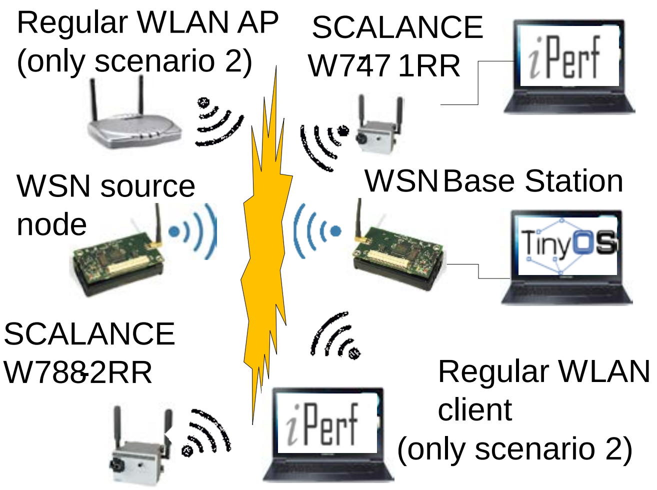

Figure 2: The experimental testbed.

- Scenario 1, Link under iWLAN interference. The iPerf-generated traffic is sent to a wireless node (Siemens SCALANCE W747-1RR) via a Siemens SCALANCE W788-2RR AP. The Siemens devices use 802.11b/g mode with iPCF enabled and the transmission set on channel 1.

- Scenario 2, Link under iWLAN and standard WLAN interference. One laptop generates traffic for the iWLAN network as in the previous scenario. Another laptop simultaneously generates traffic sent to an IEEE 802.11 AP. IEEE 802.11b/g channel 1 was used for the transmission for both iWLAN and standard WLAN networks..

a) Single codeword	*Time [ms]*
Encoding	0.29
Decoding (0 err)	0.56
Decoding (Max err)	1.77
Decoding (Uncorr.)	1.46

b) Entire Packet (Worst case)	*Time [ms]*
Encoding	2.77
Decoding	14.1

Table 1: Encoding and decoding time for an optimizied RS(15,7) implementation.

	iWLAN link	*iWLAN+WLAN link*
Packet Delivery Ratio $\mathbf{PDR} = \frac{\mathbf{N}_{\mathbf{received}}}{\mathbf{N}_{\mathbf{sent}}} \cdot \mathbf{100}$	37.50%	11.14%
Packet Salavation Ratio $\mathbf{PSR} = \frac{\mathbf{N}_{\mathbf{rec}}}{\mathbf{N}_{\mathbf{corr}}} \cdot \mathbf{100}$	1.03%	3.07%
Wrong classification $\mathbf{W} = \frac{\mathbf{N}_{\mathbf{wc}}}{\mathbf{N}_{\mathbf{corr}}} \cdot \mathbf{100}$	0.40%	1.90%
Do Nothing	0.20%	0.10%

Table 2: iWLAN and standard WLAN LPED interference classification performance

$N_{received}$ represents the total number of received packets (with a correct PHY and MAC header), N_{sent} is the total number of packets sent by the transmitter, N_{corr} represents the number of received, but corrupted packets, N_{rec} is the number of the packets successfully recovered after decoding and N_{wc} is the number of packets wrongly classified.

Single-Photon Avalanche Diodes: devices and advanced applications

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Photon counting is the technique of choice for attaining ultimate detection sensitivity in measurements of very faint optical signals at very fast (picosecond) time scale. Photon counting and timing was introduced and developed with PMTs, but widespread advanced applications are enabled by means of microelectronic detectors, namely the Single-Photon Avalanche Diodes (SPADs). SPADs exploit avalanche multiplication in a p-n junction for producing a standard current pulse with macroscopic size and fast rise-time that marks the photon arrival time with high (few ps) precision. Nowadays, silicon SPADs (both single point and arrays) and InGaAs/InP SPADs are well assessed and are commercially available, while new solutions are under development for even better performance with reduced costs and size.

We present our recent results about Silicon SPADs developed in standard CMOS technology and custom InGaAs/InP SPADs for the near-infrared (NIR) wavelength range.

CMOS SPAD imagers based on smart pixels (including counting and timing circuitry, able to count photons and to measure their arrival time) are the basis for single-photon counting and timing cameras, at very high frame rate (100 kfps), low noise (dark count rate < 100 cps/pixel with 30 µm active area diameter), and high detection efficiency (> 50%) [1]. We employed such cameras (with up to 64x32 pixels) [2],[3] in a wide range of applications, in chemistry, biology, medicine, material science, and physics, including Forster Resonance Energy Transfer (FRET), Fluorescence Lifetime Imaging Microscopy (FLIM), Fluorescence Correlation Spectroscopy (FCS), and 3D acquisitions (LIDAR). Recently, we have developed an advanced fast-gated silicon SPAD, with very fast (~ 200 ps) rising edge, in order to greatly widen dynamic range and speed-up acquisition time in time-resolved measurements, such as diffuse optical spectroscopy for brain imaging.

For extended NIR sensitivity, we have designed and developed InGaAs/InP SPADs for up to 1.7 µm. The 25 µm active-area diameter detector shows very low dark count rate (< 10 kcps at 225 K), 30% photon detection efficiency at 1550 nm, low afterpulsing, and a timing response with less than 90 ps jitter [4]. We employed our InGaAs/InP SPADs in many different applications, like eye-safe ranging (LIDAR), time-resolved spectroscopy, single-photon source characterization, fluorescence decay analysis, ghost imaging.

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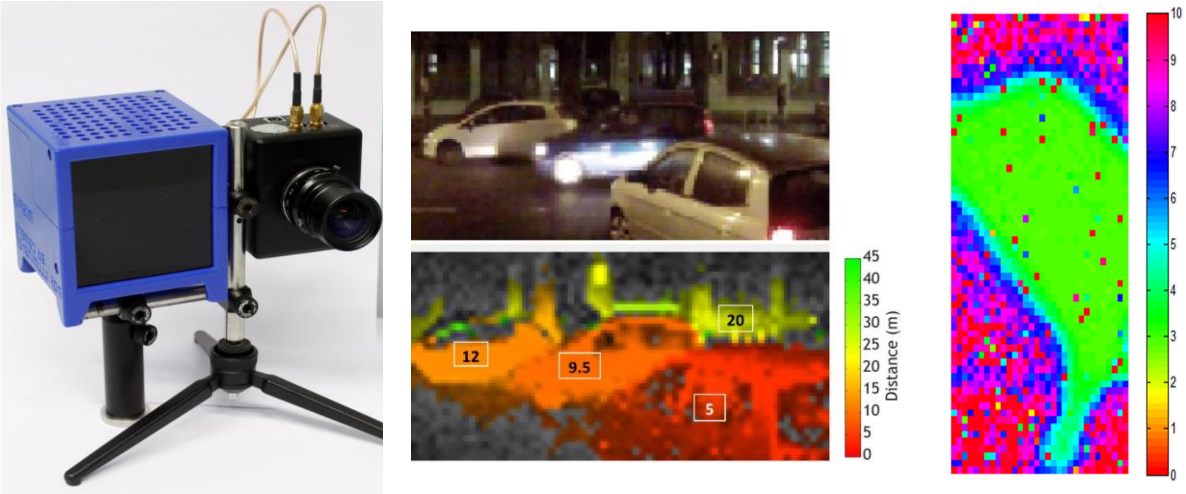

Figure 1: Left: Picture of a 64x32 SPAD camera with optics and laser illumination system. Center: Frames from a 3D movie at 100 fps acquired by the 64x32 SPAD camera: one car (in red at 5 m) is entering into a lane where another car (in orange at 9.5 m) is moving fast and a third car (in yellow-orange at 12 m) is parking. Right: Fluorescence lifetime of a transfected cell as measured by the 64x32 SPAD camera.

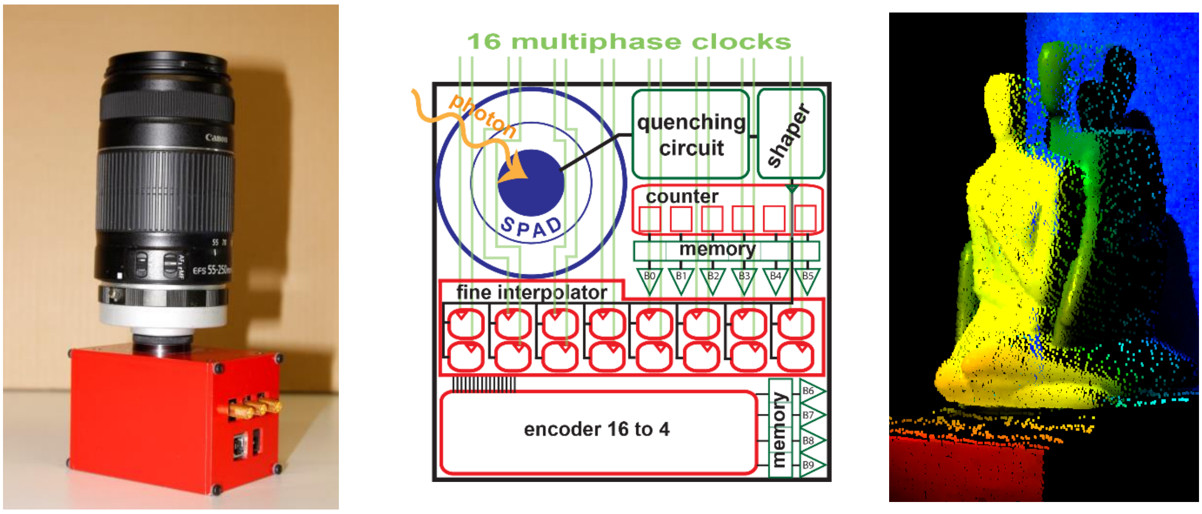

Figure 2: Left: Picture of the 32x32 SPAD camera with integrated Time-to-Digital Converters (TDCs). Center: Smart pixel of a 32x32 SPAD array in which a SPAD detector is coupled to a 10 bit TDC for measuring the time-of-flight of single photons. Right: 3D map of a 20 x 10 x 10 cm^3 statue acquired by the 32x32 SPAD camera.

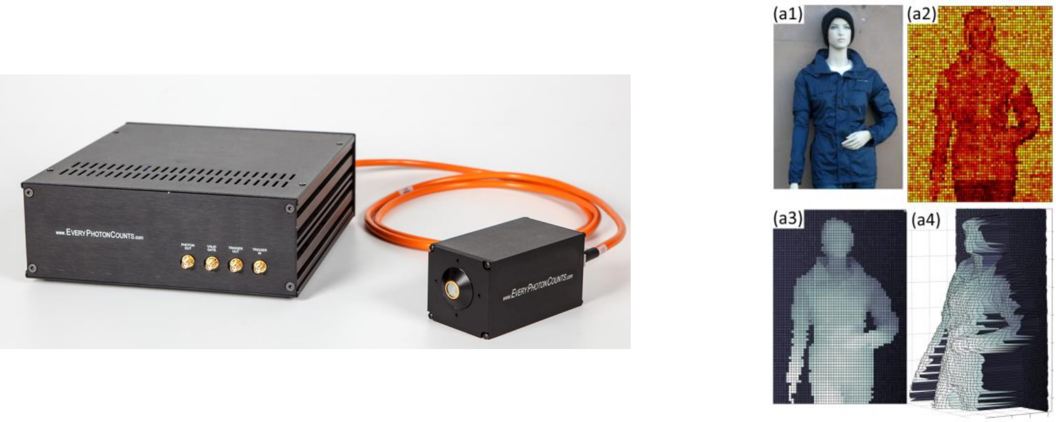

Figure 3: Left: Picture of a single photon counter based on InGaAs/InP SPAD. Right: Depth profile scan at λ = 1550 nm of a life-sized mannequin at a range of 325 m using a per-pixel acquisition time of 5 ms.

Skin-Electrode Impedance Equalization for CMRR Improvement in portable ECG System

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Electrocardiography is one of the most important diagnostic methods for heart monitoring. In order to make feasible a wearable monitoring system, much attention should be paid to the comfort of the patient. Ag/AgCl electrodes are widely used, but they present several drawbacks. Electrolyte paste or conductive adhesive are required to assure a good skin-electrode electrical contact, but they usually suffer the drying action, leading to a progressive degradation of the signal to noise ratio (SNR). Furthermore, they may cause irritation and discomfort and are a potential cause of skin allergy and inflammation. Alternatively, several authors [1–3] have developed dry electrodes that are able to acquire an ECG signal but accepting a larger noise at the inputs.

Noise is mainly due to the Electromagnetic Interferences (EMI) which are capacitively coupled to the measurement system and amplifiers with high CMRR (more than 100 dB) are commonly used since a differential acquisition channel leaves the noise uncoupled to the branches. But unfortunately the goodness of the electrode-skin contact degrades with time and introduces an asymmetry in the system, thus deteriorating the CMRR (down to 60 dB) and ultimately the SNR [4,5]. A system that compensates for these asymmetries, is potentially able to keep the CMRR to acceptable values, even in presence of a poor skin-electrode contact.

In order to improve the native SNR, an embedded system has been designed and implemented (block scheme in Fig. 1). The analog front-end is an ADS1198 (from Texas Instruments), optimized for scalable medical instrumentation systems with eight differential channels (16 bits delta-sigma ADC). Moreover the system shows two digital potentiometers (100kΩ each) in the two differential branches of a front-end channel, programmed to compensate for the skin-electrode resistances difference. Two others 10kΩ potentiometers are used instead to delete the CMRR decay due to the needed antialiasing filter and the resistance mismatch of ADS1198 channel.

Without any compensation, the CMRR of the system easily drops to around 60 dB but, by adjusting the 10kΩ potentiometers (see Fig.2), the maximum CMRR is restored to the initial value. After this compensation of the inputs circuit asymmetries, the system is now able to compensate skin-electrode impedance mismatch, measuring the resistance difference between branches and canceling it with the use of the 100kΩ potentiometers. Fig. 3 compares the obtained CMRR with that of the uncompensated system. The CMRR improvement is constant and above 18 dB, as long as the impedance difference between branches is above 2KΩ .

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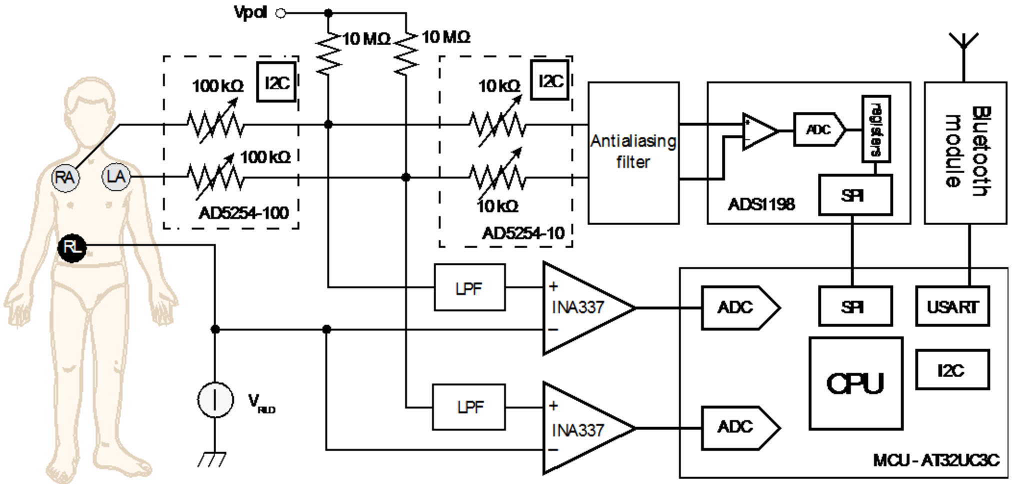

Figure 1: Simplified scheme of the implemented ECG system.

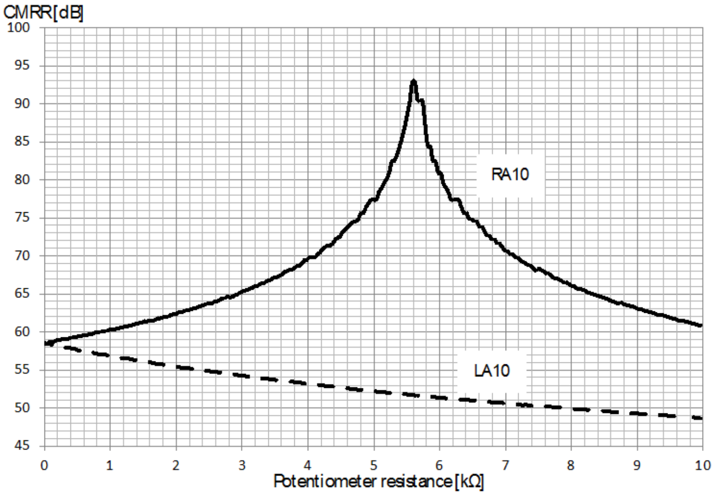

Figure 2: CMRR versus 10kΩ potentiometer values (antialiasing filter compensation).

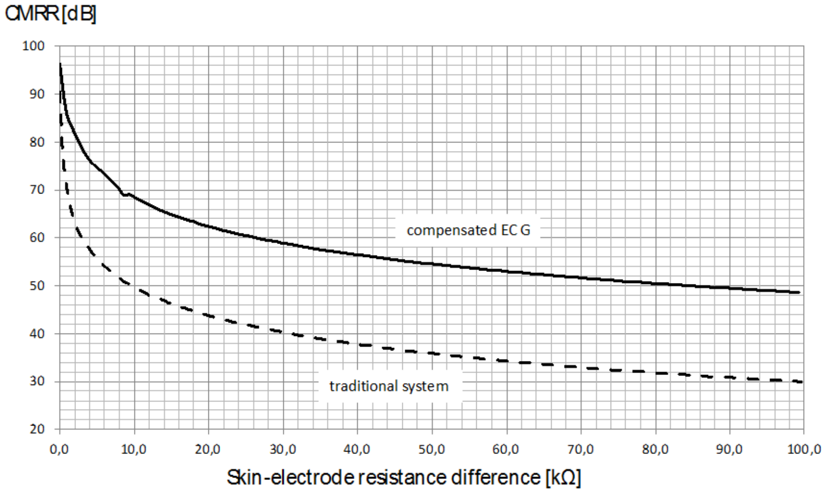

Figure 3: CMRR for the compensated system (solid) and uncompensated (dashed) versus the resistance difference of the channel branches.

Temperature sensor based on 4H-SiC diodes

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Silicon carbide (SiC) is a promising semiconductor material for extreme environment sensing applications thanks to its superior material properties, i.e. high thermal conductivity (3-5 W/cm°C), high critical electric field (Ec=2-5 MV/cm), wide energy bandgap (Eg=3.23 eV), if compared to silicon and other semiconductor materials. To date, many examples of high-temperature sensors based on 4H-SiC diodes are reported. All of these simple devices reported in literature exploit the almost-linear dependence of the forward voltage (or reverse current) on temperature, showing sensitivities as low as S=3.5 mV/°C (5 μA/°C) [1-3].

In this work, a proportional to absolute temperature (PTAT) sensor based on integrated 4H-SiC Schottky diodes is presented. The linear temperature dependence between the voltages difference across the forward-biased diodes with the temperature variation in a range from 30°C up to 300°C has been used for thermal sensing.

The equivalent circuit for the PTAT sensor is shown in Fig. 1. The Schottky diodes, D1 and D2, have been biased by two different currents, I_{D1} and I_{D2}, whose ratio, $r = I_{D2}/I_{D1}$, has been kept constant with the temperature T.

The sensor has been tested in a thermostatic oven (Galli G210F030P) setting the reference temperature through its internal PID digital microcontroller.

The voltage differences (V_{D2}-V_{D1}), for tree different consecutive measurements, in a range from (up to) 30°C up to (from) 300°C are reported in Fig.2 together with the best linear fitting. The coefficient of determination (R^2) was calculated to determine the sensor output linearity. For I_{D1}=0.5 mA and I_{D2}=1.3 mA our PTAT sensor shows a maximum level of linearity ($R^2 \approx 0.9995$) and, from the slope of the $(V_{D2}-V_{D1})$ *vs.* T characteristic, a sensitivity of 5.11 mV/°C was calculated.

Four different couples of diodes were characterized and their long-term stability tested, in order to evaluate their reproducibility and how consistently they maintain a stable output over time, by iteratively repeating the same cycles of measurement, from (up to) 30°C up to (from) 300°C, in different days.

The results are summarized in Fig. 3, and leaded to a calculated maximum r.m.s. error of less than ±1.5%. Moreover, the coefficient of determination is $R^2=0.9993\pm2\times10^{-4}$ and the corresponding sensitivity is S=5.02 mV/°C with a standard deviation of 0.18 mV/°C.

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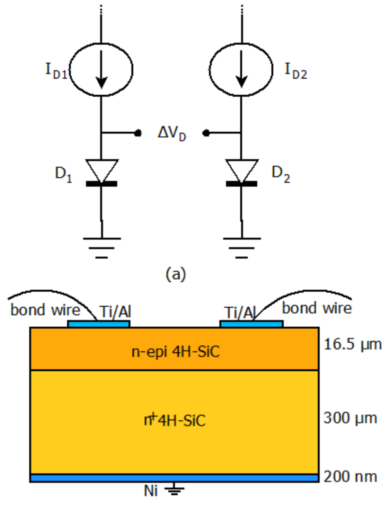

(a)

(b)

Figure 1: (a) Electrical circuit of PTAT sensor; (b) Schematic cross section of integrated 4H-SiC Schottky diodes.

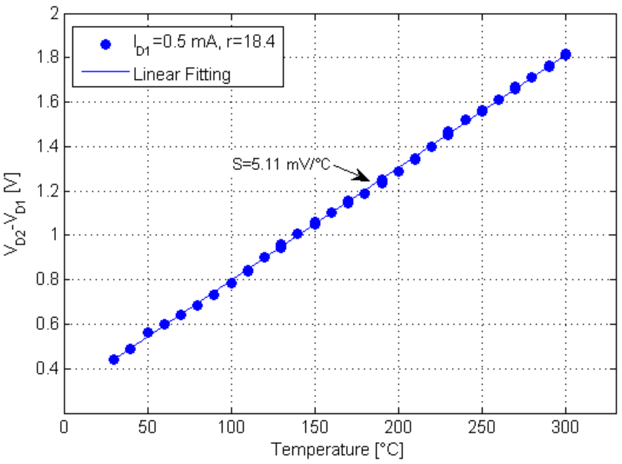

Figure 2: Voltages difference *vs.* temperature for bias currents I_{D1}=0.5 mA and I_{D2}=9.2 mA.

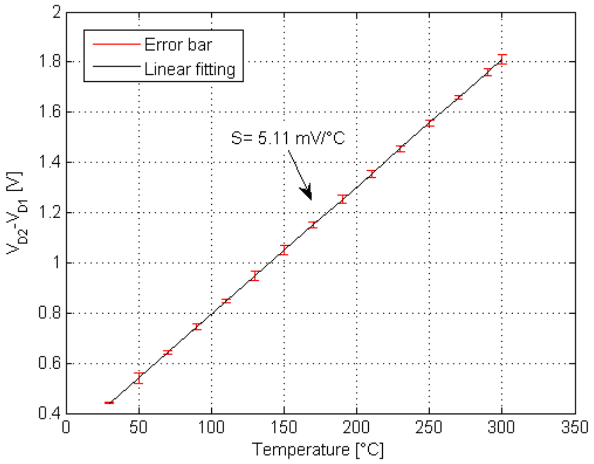

Figure 3: Linear fit and r.m.s. error of (V_{D2}-V_{D1}) *vs.* T for four sensor pairs. The measurement cycles, from (up to) 30°C up to (from) 300°C, were done in different days. The bias currents are the same for all the PTAT sensors, I_{D1}=0.5 mA and I_{D1}=9.2 mA.

Towards Social Serious Gaming in the IoT Concept and Prototype Development

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The Internet of the Things (IoT) requires designing and exploiting cyberphysical systems, that are able to digitalize and manage real-world physical processes, allowing digital data capture, storage, control and processing. From an architectural point of view, this means development of systems based on cloud computing, service oriented architectures and big data processing.

The paper addresses user performance analytics for car driver performance. We focus on descriptive analytics and our approach relies on educational serious games, in order to improve the driver's behavior (in particular concerning green driving) in a pleasant and challenging way. We propose a general IoT social gaming platform (SGP) concept that should be adaptable and applicable to any kind of application domain. The distributed platform includes three layers: the field devices, the cloud servers and the user personal devices, as illustrated in Fig. 1.

Fig. 2 represents the IoT SGP implementation in the automotive domain, as we are developing it in TEAM. We are developing two main kind of social gaming services:

- Virtual coin service, a sort of virtual bank where users can accumulate coins won through good performance in different apps and spend on real-world items (e.g., bus tickets, parking lots tickets etc.) and on acquisition of better level of services in the different apps as well.
- Competition management, including: self and social comparisons; periodic (time and space-based) competitions; several different apps can be aggregated in competitions; game features (Charts, comparison and ranking, badges); feeds to the Virtual coin server

Fig. 3 shows the details of the virtual sensor that we are developing in vehicles in order to analyze the user's green-drive behavior. This sensors exploits different algorithms processing the vehicular signals (e.g., speed, position, pedal activity, fuel consumption, etc.) accessed through a gateway to the car CAN network. The algorithms include:

- Linear distances. Comparison with ideal linear functions (single signals by now), in a sample by sample evaluation suited for immediate feedback
- Dynamic sliding windows. Recognition of significat windows of signal values, with detection of events, thus suited for event-based feedback and coaching
- Kohonen neural network. Unsupervised learning, with classification of signal patterns into clusters and recognition of events in batches of 2-5 minute length.
- K-nearest neighbors. Supervised learning, with a sample by sample classification, thus suited for immediate feedback and coaching

A supervised learning neural network is under development as well.

We are now evaluating and tuning the algorithms by processing data recorded on a FIAT 500L vehicle that is being driven by different users in a test path on different kinds of roads in the Trento areas. Preliminary results are promising about the possibility of processing data in real-time in order to have a continuous evaluation of drivers for gaming and coaching purposes.

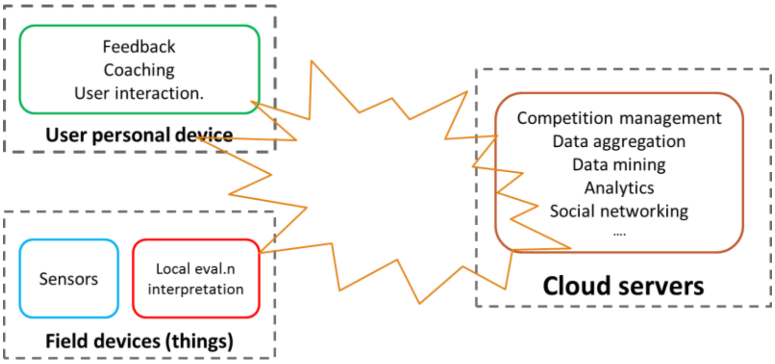

Figure 1. The IoT Social Gaming Platform concept

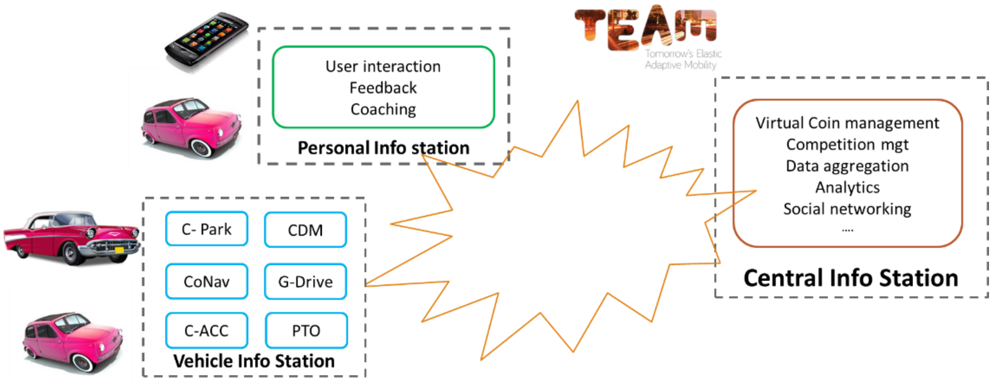

Figure *2*. The IoT SGP TEAM implementation in the automotive domain, with different apps – developed exploiting vehicular and other mobility information – contributing to the player performance evaluation, thus enabling the game dynamics

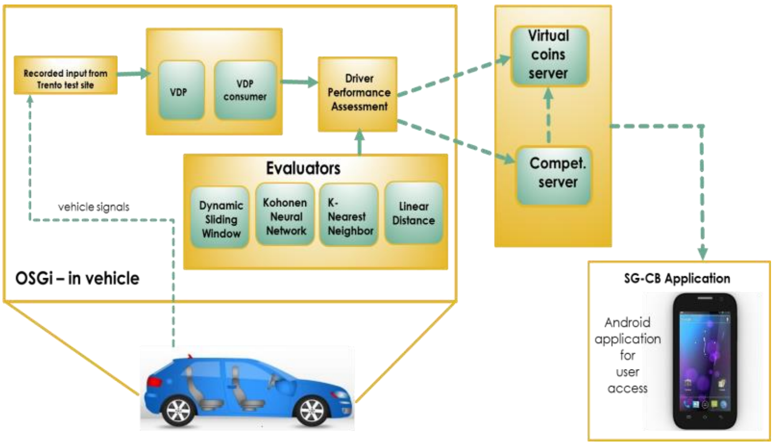

Figure 3. The green drive system architecture being developed in TEAM

ULA-OP 256: a modular high-performance research platform for ultrasound[1]

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The development of ultrasound open platforms presents significant challenges in the area of electronic system design. Such systems must be highly programmable and have huge computational power to allow developing novel methods for the next generation of echographic instruments. Furthermore, their dimensions should be limited, to allow the transportability to other laboratories, and the power budget must be accordingly considered.

This paper describes the development of a 256-channel ULtrasound Advanced Open Platform (ULA-OP 256), designed to be able to control a large class of ultrasound probes having up to 256 active elements. A modular approach was adopted. The architecture is based on multiple 32-channel front-end (FE) modules. Each FE module integrates all the electronics to manage the transmission (TX), reception (RX) and real-time elaboration for 32 channels (Fig. 1). An on-board FPGA (ARRIA V, Altera) is in charge of generating 32 independent TX analog signals with frequency up to 25MHz. The same FPGA receives the 32 ultrasound echo-signals amplified and digitized at 80Msps with 12-bit resolution by four 8-channel ultrasound front-end ICs (AFE5807, Texas Instruments). The digitized signals are “beamformed” in real-time inside the FPGA. Two 8-core DSPs (TMS320C6678, Texas Instruments) hosted by the same FE board are in charge of receiving the beamformed data and applying coherent demodulation, filtering and/or custom elaboration modules.

All FE modules are connected one to each other through a SerialRapidIO (SRIO) channel routed on a backplane (Fig. 2). The interconnection topology was chosen to be a ring, where each communication interface runs at a raw data rate of 40Gbit/s (8 lanes at 5Gbit/s) full-duplex. The FE module has two interfaces, one for each side of the ring, thus bringing a total data rate of 80Gbit/s. Each onboard computing device (either DSP and FPGA) is interconnected to any other in the system through the SRIO link. On the entire system, with 8 FE modules installed, a total of 64GB of DDR3 memory (expandable up to 128 GB) is available. This huge memory allows storing significant amounts of RF raw data, post beamformed RF data or demodulated (baseband) signals. The cumulative processing power of the installed DSPs is 5000GMAC or 2500GFLOP. This will allow the implementation of novel signal elaboration techniques like high frame rate imaging and real-time vector Doppler.

A first prototype system connected to a host PC by an USB 3.0 SuperSpeed link has been assembled and is currently tested in our laboratory. A massive parallel multi-line beamformer was implemented inside the FE FPGA in order to speed up the elaboration in high frame rate imaging techniques. The beamforming power inside the FPGA allows to generate echographic images at up to 4000 fps.

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[1] This work was supported by the Italian Ministry of Education, University and Research (PRIN 2010–2011)

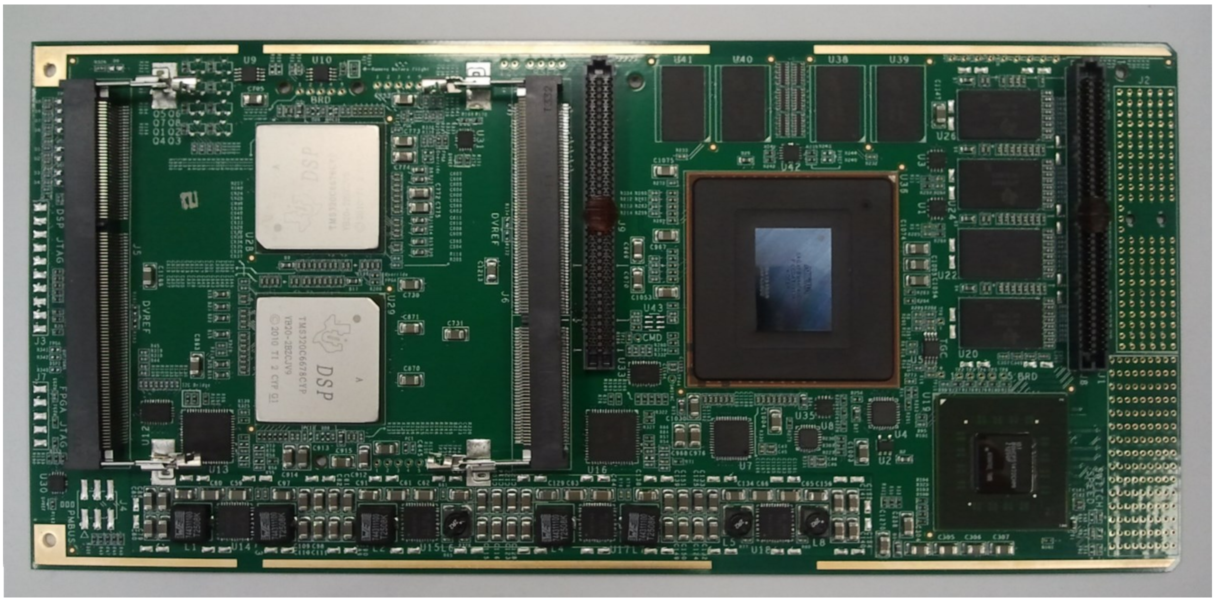

Figure 1: FE module board.

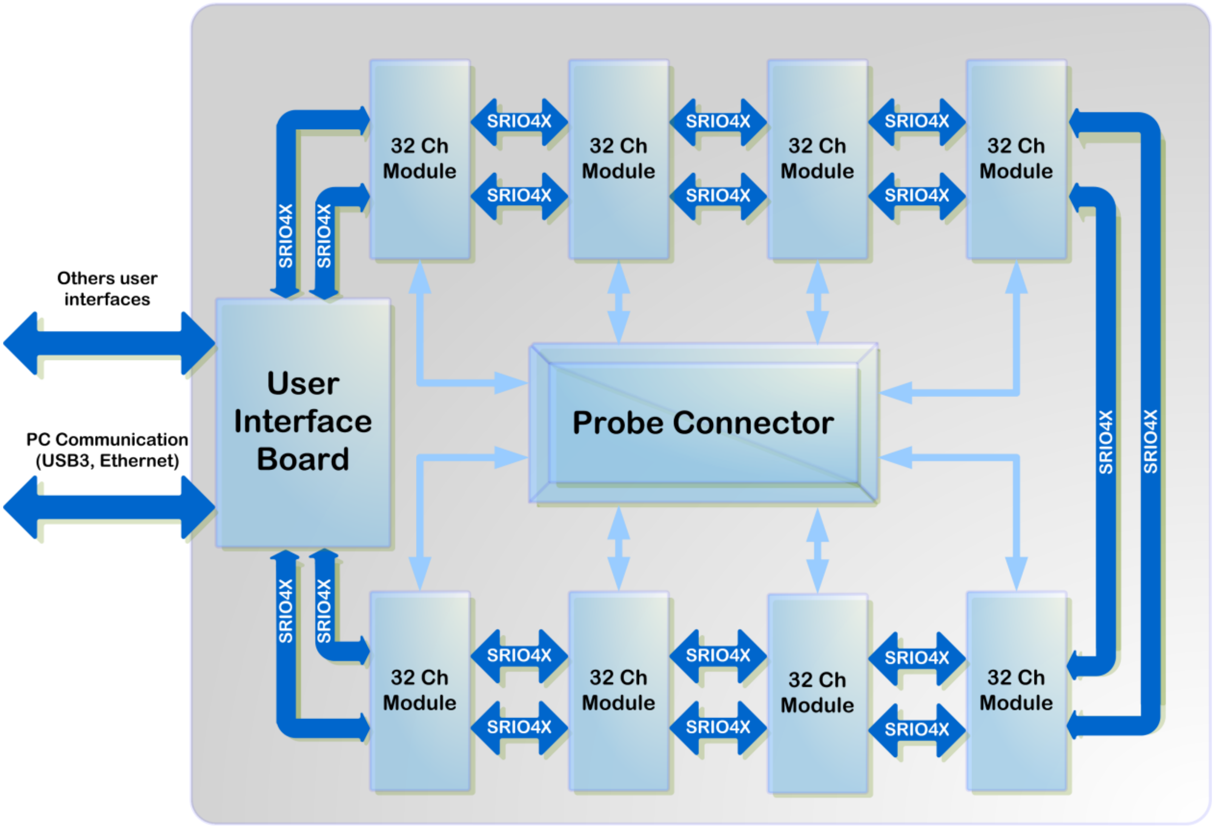

Figure 2: FE module board.

Ultrasound Imaging for Biometric Recognition through 3D Hand Geometry

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Ultrasound has several specific advantages over other technologies in the field of biometric recognition, including the capability to provide information not only of the skin surface but also of the under skin volume and the not sensitivity to surface contaminations like stain, dirt, oil, ink. Some of the authors have recently proposed and ultrasound technique for extracting and evaluating different biometric characteristics including Palmprint [1], [2]. In this work, an ultrasound technique able to acquire the 3D Hand Geometry is presented.

Figure 1 shows a photo of the experimental setup used to get 3D ultrasonic images of the human hand. The palm of the user is placed on a plastic jig, which has guidance marks on it. The hand is properly aligned by the marks and is completely immerged in water with the palm facing upwards. The human palm is illuminated by an ultrasonic probe, which is connected to an ultrasound imaging system. The ultrasonic probe is a commercial 192 elements linear array by Esaote S.p:A., Genova – ITALY, model LA435. It has a central frequency of 12 MHz with a bandwidth of about 75%. It is partially immersed in order to be faced and acoustically coupled to the hand palm. The probe is mechanically shifted along the elevation direction by means of a numeric controlled pantograph by Delta Macchine CNC, Vazia (RI) – ITALY, which is able to guarantee a precision better than 20 μm. As ultrasound imaging system an advanced open platform for ultrasound research (ULA OP) was employed [3]. The system is characterized by the full programmability of each critical section and allows to implement TX-RX strategy to control simultaneously a maximum number of 64 elements. Both the pantograph and ULA OP are controlled in MATLAB environment (The MathWorks, Inc., MA, USA).

In order to investigate and acquire ultrasound images of the whole human hand, five linear parallel mechanical scans have been performed. The adjacent scans are partially overlapped to guarantee an effective continuity. To make the acquisition process very fast (about 40 s), the whole VOI is acquired in a single record; the overlapped volumes are then realigned offline and fused using a convex combination, which weights follow a raised cosine law. This operation is necessary since the movement of the probe and the acquisition of the signals are completely asynchronous.

Fig. 2 shows a 3D rendering of the ultrasound image acquired from an user. Note that it can be exploited to extract simultaneously 3D Hand Geometry and 3D Palmprint.
Fig. 3 shows a 2D view of the ultrasound image. The quality of the image allows to take all the measurements used for the template definition in the 2D cases.

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Figure 1: A photo of the experimental setup.

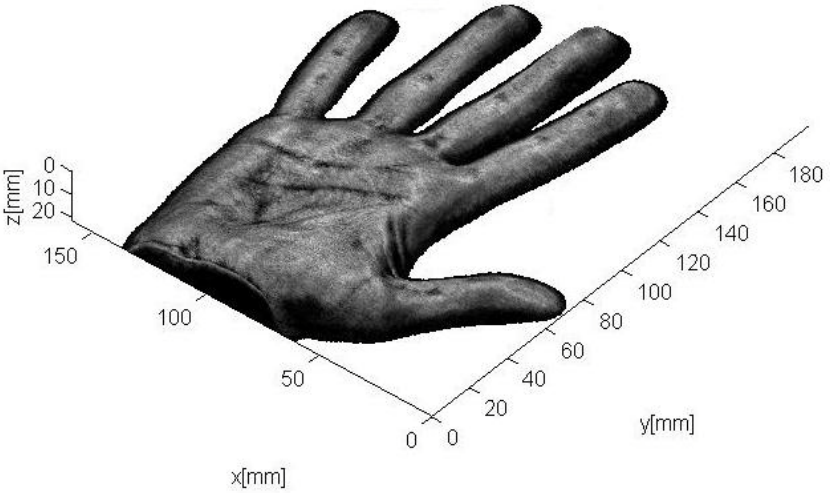

Figure 2: 3D rendering of a human hand.

Fig. 3. The ultrasound image with some of the measurements taken in the classical Hand Geometry recognition method.

Voice Activity Detection System for Power Saving in Audio Wearable Devices

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Power consumption is often one of the most important constraints of embedded devices. A Voice Activity Detection (VAD) algorithm can improve device battery life because data processing can be done only when user talks. In such way, the number of instruction needed for audio processing can be reduced and the embedded CPU can be put in low power mode, improving power consumption performances.

MEMS digital microphones could be very attractive for an audio embedded device due to their small size, cost and performances. However, they require additional processing to decode Pulse Code Modulation (PCM) samples from Pulse Density Modulation (PDM) ones, increasing the number of Mega Instructions per Second (MIPS) required by the application.

In literature do not exist a VAD algorithm that uses PDM data, so decoding samples is a necessity also when user's voice is not present, and this requires additional clock cycle and power consumption.

In order to run PCM to PDM conversion routine only when needed, we have designed an hardware/software first order Cascaded Integrator-Comb (CIC) Filter [1] to obtain Pseudo-PCM samples, using two timer peripherals of a Cortex M4 CPU.

In Fig.1 is shown the schematic block diagram of the filter.

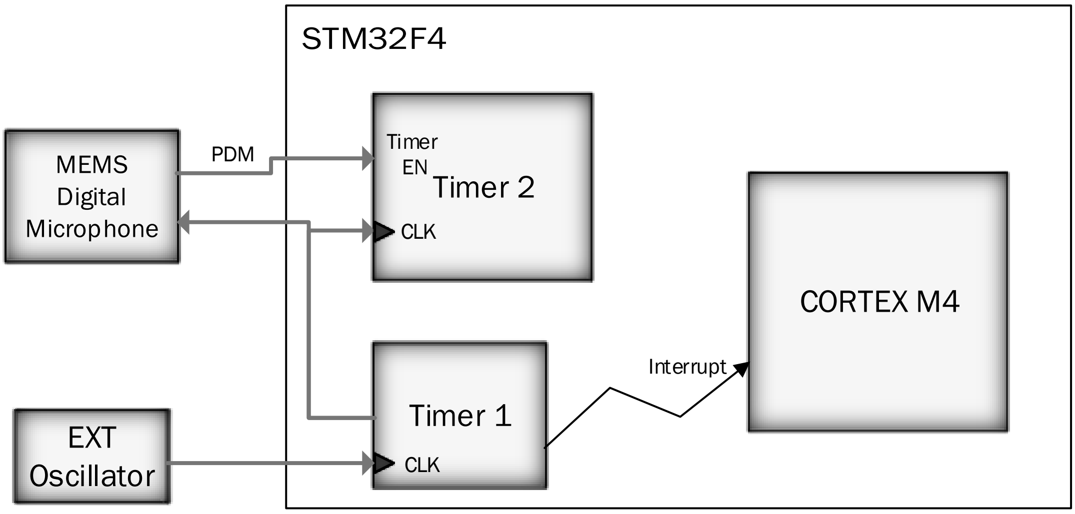

Figure 1: VAD block diagram

The Timer1 provides the microphone clock from an external oscillator and generates an interrupt every 20 ms. The PDM data from the microphone feed the enable pin of the Timer2 peripheral. In such way Timer2 works as an accumulator. The Timer1 ISR implements the Comb part of the filter as a software routine.

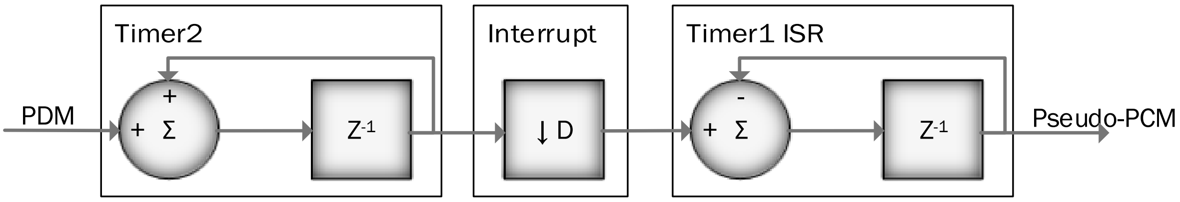

Figure 2: HW/SW CIC decimator Filter

Any standard VAD algorithm [2] [3] [4] can use the Pseudo-PCM data as an input, even if their quality in terms of SNR are lower than true PCM samples. The proposed system has been evaluated comparing with a standard time domain VAD algorithm [2] in terms of MIPS, Power Consumption, Precision and Recall [5] (for every 20 ms frame. This measurement has been done using an STM32F407VG with $f_{clk} = 168\ MHz$.

	MIPS	Power Consumption	Precision	Recall
SW VAD	0.52	1.25 mA	92.3%	87.4%
HW/SW VAD	0.15	0.432 mA	91.7%	85.0%

Finally in Fig. 3 is shown the VAD activation threshold in terms of dB SPL (Sound Pressure Level).

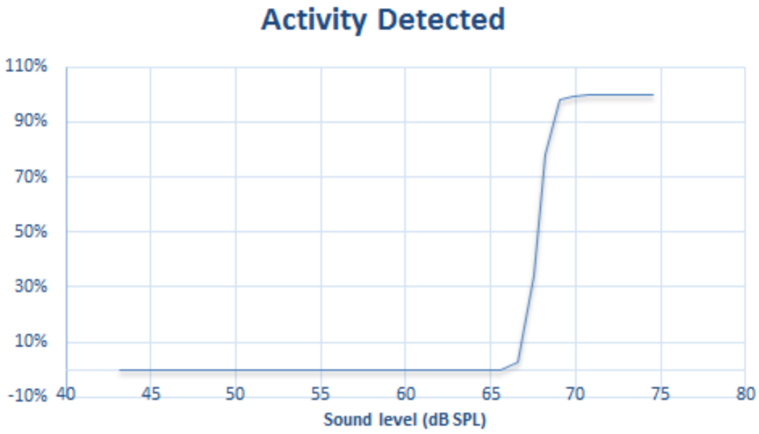

Figure 3: Audio Activity Threshold

In conclusion the proposed system can improve the overall power consumption of an embedded wearable audio device. Anyway, due to the reduced quality of Pseudo-PCM data, the system decreases voice detection Precision and Recall features.

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1.2-V supply, 16-bit ΣΔ Modulator in 90-nm CMOS technology

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The abstract presents the design and implementation of a low-power, 3rd order, switched-capacitor (SC) sigma-delta (ΣΔ) modulator in STM 90-nm CMOS technology, Fig. 1. This is one of the first implementation in 90-nm technology achieving a resolution of 16-bit over a signal bandwidth of 250-Hz at 1.2-V.

The project was developed by means of an accurate behavioral model implemented in SIMULINK and specifically designed for ultra-low power ΣΔ modulator [1]. The systematic design follows the steps in the flow-chart of Fig. 2 and exhibits an iterative approach. The reverse feedback path in Fig. 2, corresponds to the simulation process. At the lowest level of the flow-chart, simulations, being transistor-level, require a huge CPU time. For this reason the accuracy of the behavioral model is mandatory to speed-up the design process. State-of the art models [3] neglect some second-order effects which have a significant impact on the modulator performance in a ultra low-power oriented design. Thanks to the higher accuracy of the proposed model, the number of design iterations requiring transistor-level simulation is minimized. In particular, the voltage discontinuity occurring at the beginning of the integration phase in the circuit of Fig. 3 has a detrimental effect on the harmonic distortion at the modulator output. Moreover, the input differential-pair of the op-amp in Fig. 3 exhibits a variable small-signal transconductance. Both effects are included in the proposed model.

The implemented modulator exhibits a silicon area of 0.4-mm^2; the chip photograph is in Fig. 4. Measured SNR and signal-to-noise-and-distortion ratio (SNDR) Vs. the input signal amplitude are shown in Fig. 5. It has worth noticing that measurement results are in good agreement with both transistor-level and behavioral-model simulations. A comparison with 3rd order ΣΔ modulators at the state-of-the-art is reported in Table 1. The considered designs exhibit similar architectures: low-pass single-loop with single-bit quantizer. In all cases, the main features of each reported design are summarized in terms of the following performance metrics: signal bandwidth (f_B), oversampling ratio (OSR), supply voltage, CMOS technology process, power consumption, dynamic range (DR), peak signal-to-noise-and-distortion ratio (SNDR) and SNR. The comparison was carried out in terms of Figure-of-Merit (FOM).

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Ref.	f_B [kHz]	OSR	Supp. Volt. [V]	CMOS Tech.	Power [uW]	DR [dB]	Peak SNDR [dB]	Peak SNR [dB]	FOM [pJ/cov]
[4]	25	100	1	0.35-um	950	88	85	87	0.88
[5]	20	100	1	90-nm	140	88	81	85	0.18
[6]	50	65	0.65	90-nm	27	65	59.5	61	0.19
This work	0.25	500	1.2	90-nm	50	98	92.5	94	1.5

Table 1: Performance comparison.

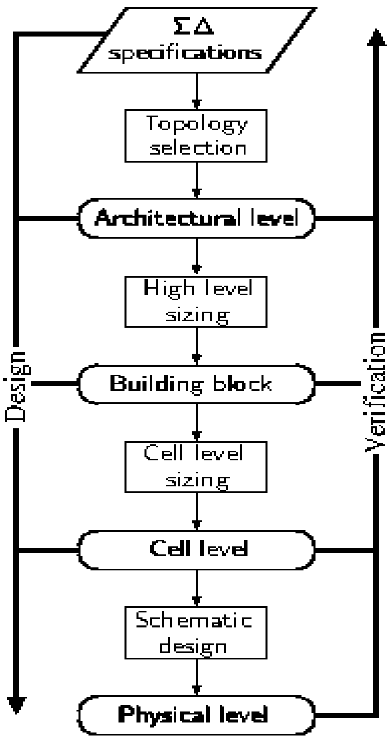

Fig. 2: ΣΔ modulator design flow-chart: from behavioral model to physical level

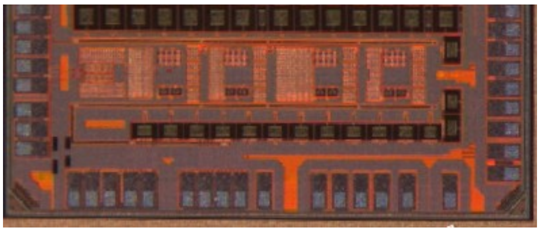

Fig. 4: chip photograph.

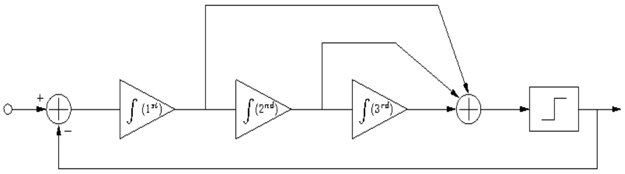

Fig. 1: 3rd order ΣΔ modulator black-box schematic.

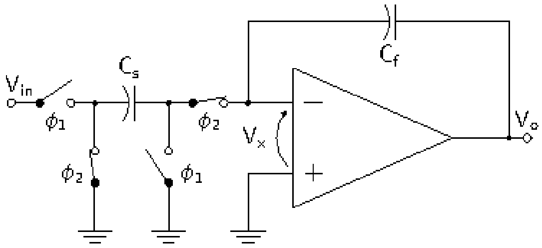

Fig. 3: SC integrator schematic (single-ended equivalent).

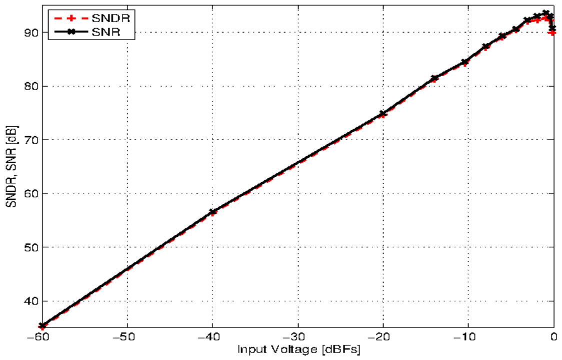

Fig. 5: measured SNR and SNDR vs. input amplitude (referred to the voltage reference)

A 25-Gb/s FIR Equalizer Based on Highly Linear All-Pass Delay Line Stages in 28-nm LP CMOS

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To address demands for pushing speed of serial links, new 25-28 Gb/s standards are emerging. Inter-symbol interference (ISI) is a severe obstacle and transceivers need sophisticated channel equalization techniques. RX equalization combines a feed-forward equalizer (FFE) and a decision feedback equalizer (DFE). FFEs implemented as FIR filters, have been recently proposed [1-2]. They provide high flexibility to match the channel response and are compatible with simple adaptation schemes. This abstract presents a 25-Gb/s 4-tap FIR equalizer in 28-nm LP CMOS [3]. To keep high SNR and not compromise equalization performances, a new all-pass stage is proposed to realize a continuous-time delay line accommodating large input signal amplitude. Measurements at 25 Gb/s prove widest opening and record power efficiency compared to state of the art.

The FIR equalizer block diagram is shown in Fig. 1. The active delay line is realized with the cascade of three stages providing a tap-to-tap delay T_d while the tap amplifiers are transconductors with a programmable gain. The transfer function $H(f) = V_{out}/V_{in}$ is given by:

$$H(f) = \sum_{i=0..3} c_i \cdot e^{-j(2\pi f \cdot i \cdot Td)}, \tag{1}$$

where $c_i = g_{mi}R_L$. Being $|c_i|$ bounded, boost at high frequency is traded for low frequency gain and output amplitude and, due to the filter noise (n_{out} in Fig. 1), large V_{in} is required to preserve SNR. As an example, the equalization of a backplane with ≈ 20dB loss at Nyquist with $|c_i| <0.6$ determines a low frequency loss of 17dB. As a consequence, with $n_{out} = 1.5mV_{rms}$ the equalizer needs $V_{out} \geq 100mV_{pk\text{-}pk}$ for SNR ≥ 30dB, corresponding to $V_{in} \geq 700mV_{pk\text{-}pk}$.

To accommodate high input swing, a new delay stage is introduced. Fig. 2 shows two block diagrams providing a first order all-pass response. The solution in Fig. 2(a) has been recently exploited in a 25Gb/s FIR equalizer for multi-mode fibers [4]. The alternative in Fig. 2(b), where a high-pass filter replaces the low-pass filter, is investigated in this work. When considering the transistor level realization, shown in Fig. 3, such architecture provides a remarkable improvement in the maximum allowed signal swing (9 dB) confirmed by theory, simulations and measurements.

Prototypes of the equalizer, fabricated in 28-nm CMOS LP from STM accommodate up to $900mV_{pk\text{-}pk}$ input swing with 1V supply and 25mW dissipation. Experiments successful prove recovery of 20dB channel loss at 25Gb/s with 50% horizontal eye opening at $BER=10^{-12}$. Chip photograph, output eye diagram and the bathtub are shown in Fig. 4. Experimental results are summarized in Table 1 and compared favorably against state of the art.

References

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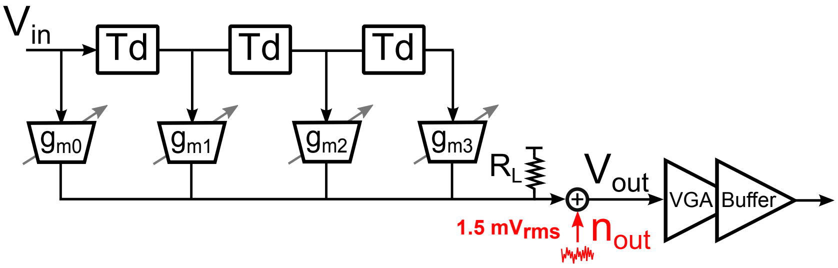

Figure 1: Block diagram of the FIR equalizer

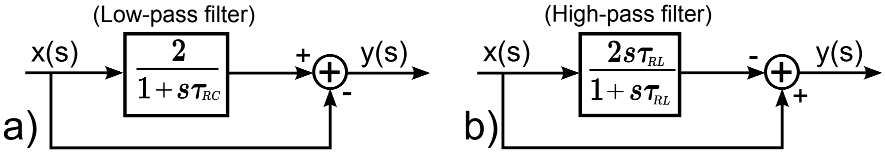

Figure 2: Block diagram of two all-pass stages

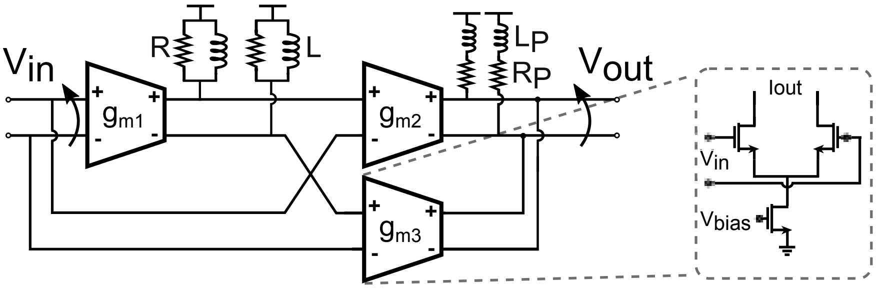

Figure 3: Schematic of the all-pass delay-line stage

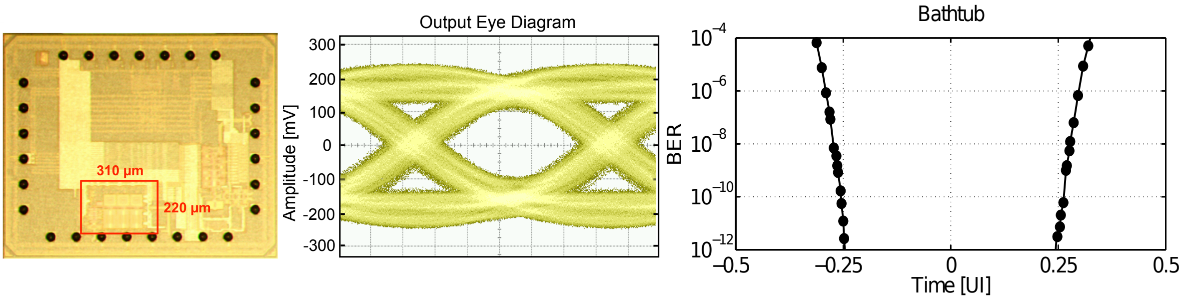

Figure 4: Chip photograph, 25-Gb/s eye diagram at the output of the equalizer and measured bathtub

Table 1: Performance summary and comparison

	This work	[1]	[2]
CMOS node	28nm LP	45nm SOI	65nm
Supply	1 V	1.1 V	1.6 V
# of Taps	4	4	3
Data Rate	25 Gb/s	17 Gb/s	40 Gb/s
Attenuation @ Ny	20 dB	21 dB	19 dB
BER	10^{-12}	10^{-9}	10^{-12}
Horizontal Opening	50%	39%	≤30%
Power Dissipation	25 mW	32 mW	55.2 mW
Power/DataRate	1 mW/Gb/s	1.9 mW/Gb/s	1.4 mW/Gb/s

A $4.4\cdot10^{-3}$-mm^2 195-nW 1-V supply Subthreshold CMOS OTA Driving up to 200 pF load

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Subthreshold design techniques, suitable are becoming more popular in the implementation of analog building blocks powered from sub 1-V supplies and with current consumptions in the order of few hundred nanoamperes. The schematic of the proposed amplifier with MOS devices operated in subthreshold is illustrated in Fig. 1. A folded-cascode amplifier M1-M8 with *p*-channel pair is used as the first stage. The second inverting stage is made up of common source M9 (and M10). The last non-inverting stage is realized by M11-M14 (note that M14 implements an additional feedforward transconductance).

We developed a design strategy aimed at setting the gain-bandwidth product as

$$\omega_{GBW} = \frac{1}{2nV_T}\frac{I_T}{\sqrt{C_{C2}C_L \tan\Phi\left(2 + I_2/I_1\right)}} \tag{1}$$

where I_T is the total bias current, being the *i*-th stage current I_i. Φ is the phase margin, C_L is the load capacitance and C_{C2} the compensation capacitance in Fig. 1. Finally, *n* is the subthreshold slope in the I-V equation.

Fig. 2 shows the die micrograph. Measured step response to a 2.5-kHz 100-mVpp input step of the OTA in unity gain and the loop-gain frequency response (C_L equal to 200), is illustrated in Fig.3. The main OTA performance parameters are summarized in Table 1. GBW is 20-kHz and phase margin is 54° and increases for lower C_L values. In order to coherently compare the other performance parameters, we adopt the two figures of merit (FOMs) in (2)-(3).

$$FOM_S = \omega_{GBW}C_L/I_T \tag{2}$$

$$FOM_L = SR\cdot C_L/I_T \tag{3}$$

The FOMs values are reported in Fig. 4. It is apparent that the proposed OTA outperforms the other previously reported solutions, irrespectively of their operation mode.

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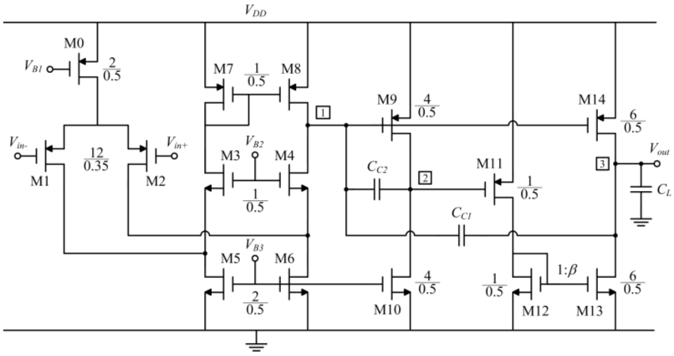

Figure 1: Simplified schematic of the amplifier.

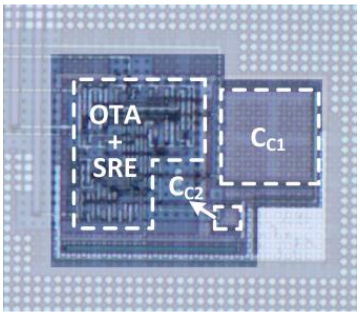

Figure. 2:. Microphotograph of the fabricated amplifier. Area is 4.4 10^{-3} mm^2.

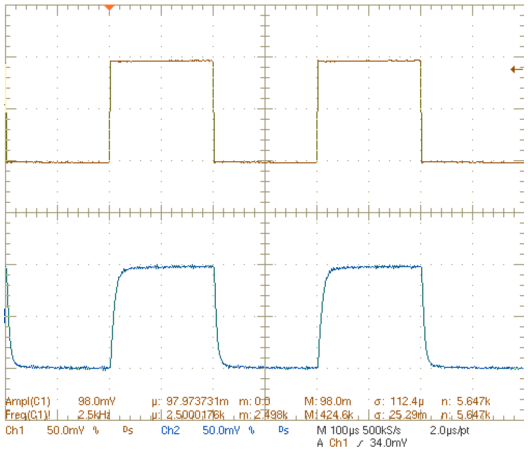

Figure 3: Measured unity-gain transient response for C_L=200 pF.

.Performance parameter	Value
Power Supply (V)	1.0
Loading Capacitance (pF)	200
DC Power Consumption (nW)	194.5
Area (mm^2)	$4.4 \cdot 10^{-3}$
DC Gain (dB) [a]	>120
Gain Bandwidth Product (kHz)	20.14
Phase Margin (deg)	54
Gain Margin (dB)	10.4
CMRR @DC (dB) [b]	70
PSRR +/- @DC (dB) [b]	70/100
Input referred noise @1 kHz (µV/√Hz) [b]	4.85
Pos./Neg. Slew Rate (mV/µs) [c]	7.38/-2.88
Pos./Neg. 1% Settling Time (µs) [c]	21.22/29.92

Table 1: OTA Main performance; [a] extrapolated; [b] post layout simulation; [c] in unity-gain.

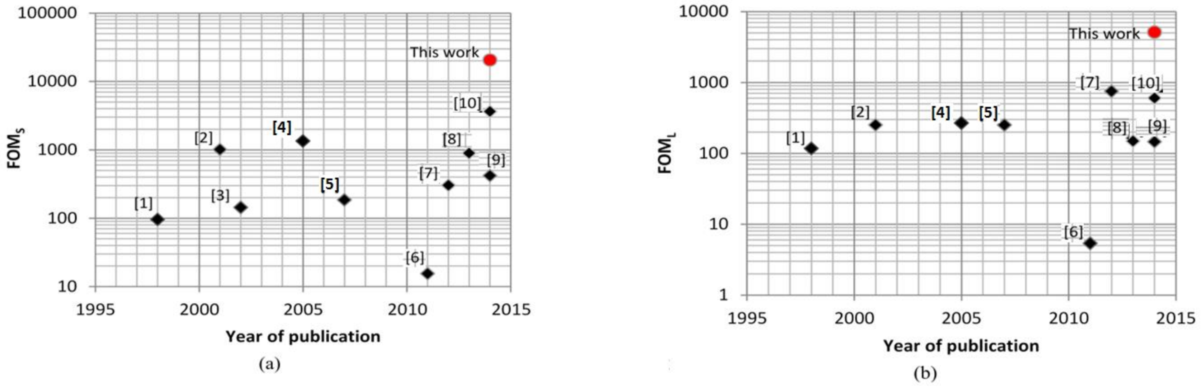

Figure. 4: Comparison with the state of the art;

a: FOM_S,

b: FOM_L ([3] not available)

A 40–67GHz Power Amplifier with 13dBm P_{SAT} and 16% PAE in 28nm CMOS LP

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The demand for high data rate short-range mm-wave wireless links is growing rapidly [1]. A wide bandwidth allows these systems to employ simple modulation schemes, considerably reducing the complexity of the front-end and cutting time-to-the-market. CMOS is the technology of choice for cost reasons, but the low gain and poor quality factor of passive components make it challenging to generate broadband power at mm-wave frequencies. Even in ultra-scaled CMOS technologies, the limited increase in cut-off frequency is counteracted by a lower quality factor of passive components resulting from the scaling of the Back End of Line. As a result, most published mm-wave power amplifiers (PAs) have relatively narrow bandwidth [2], not adequate for applications such as IEEE802.15 or Wigig.

To overcome this problem, coupled resonators in Fig.1 is adopted in this work to achieve wide bandwidth without sacrificing gain. The capacitance C1, that represents the output parasitic of preceding stage, is resonated out by inductor L1, while inductor L3 resonates out the capacitance C3 of following stage. L2 separates C1 and C3 for wideband operation. Compared to simply resonating the two capacitors by means of an inductor at center frequency, coupled resonators offer more than 2 times larger gain-bandwidth product.

Furthermore, in order to enable a compact layout to minimize parasitics, particularly critical at mm-wave frequencies. Topological transformations are employed to include a transformer for differential to single-ended conversion, to achieve the desired impedance matching and to minimize the number of components.

Using the proposed techniques, a PA prototype has been fabricated in 28nm bulk CMOS LP process [3]. Fig. 2 shows the die photo of the chip. The chip occupies an area of 620x540μm^2, pad limited. The core area is 470x120μm^2.

The measured S-parameters of the PA are shown in Fig. 3. The PA achieves a peak gain of 13dB with a 3dB bandwidth of 27GHz extending from 40GHz to 67GHz. The measured stability factor of the PA is also greater than unity for all frequencies, thereby ensuring the stability of the amplifier. Fig 4 shows the measured gain, output power and power added efficiency (PAE) of the PA at 50GHz. The PA achieves a saturated output power of 13dBm with a PAE of 16%. The measured P_{1dB} at 50GHz is 12dBm.

To sum up, this work presents a design technique for ultra wideband matching networks of PA. The fabricated prototype demonstrates state-of-the-art performances over the widest reported fractional bandwidth.

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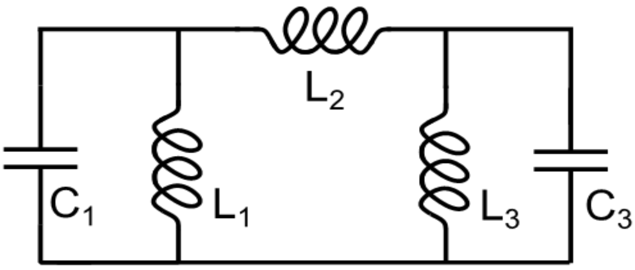

Figure 1: Coupled resonator.

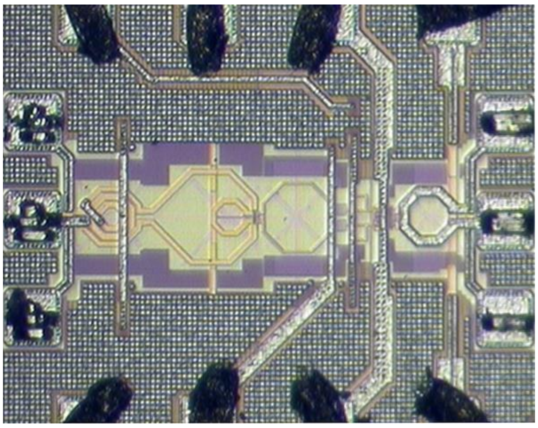

Figure 2: Microphotograph of the chip.

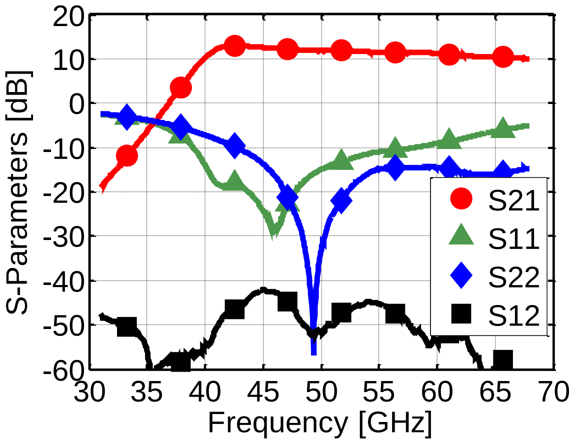

Figure 3: Measured S-parameters.

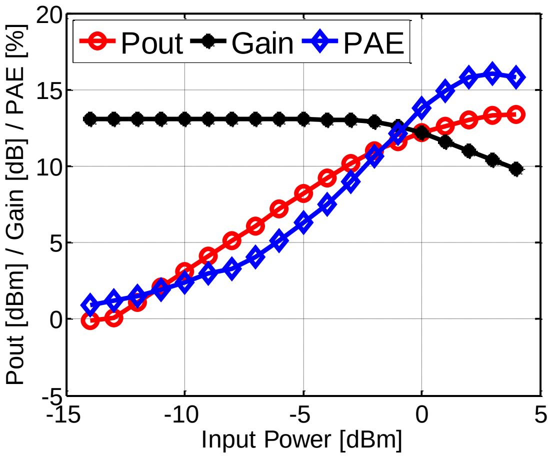

Figure 4: Measured gain, output power and power-added efficiency at 50 GHz.

A CMOS bioelectronic interface for neural recording and stimulation applications

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The recent advancements in neuroprosthetics have pushed forward the development of new implantable electronic interfaces between the Peripheral Neural System (PNS) and a robotic limb [1]: in this paper a system realizing a bidirectional neural interface is presented. The system comprises two custom designed Integrated Circuits (IC), one implementing the recording unit and the other implementing the stimulation unit. An hermetic package was also conceived and designed to host the ICs in order to make the proposed system implantable, as shown in Fig. 1.

The recording chip, realized with the AMS 0.35µm technology, includes eight acquisition channels each one composed by a Band Pass Filter (BPF) with a gain of 40 dB in the signal bandwidth (800 Hz – 8 kHz) and a third order Sigma Delta Modulator (SDM) realizing the Analog to Digital conversion. The input signals are capacitively coupled to the system trough a 40 pF capacitor resulting in a 4 MΩ input impedance @ 1 kHz. Moreover, the low cut-off frequency of the BPF is digitally tunable in the range 100 Hz – 1 kHz with no need of external components. The Input Referred Noise of the recording chain was measured to be approximately equal to 2 μV_{rms}: Fig. 2 shows a sample of the recorded noise obtained with the input shorted to ground.

The stimulation chip, implemented in the AMS HV 0.35µm technology, includes eight stimulation channels that are able to output a current whose value could be varied digitally in the range 10 – 320 µA. The impedance at the electrode-tissue interface is highly variable and degrades with time, therefore a high voltage supply is needed to guarantee the selected stimulation current even in case of high impedance contact [2]. For this reason, a voltage booster has been introduced in the design to provide a high voltage supply to the stimulator output stage. Fig. 3 shows how a supply voltage up to 15.8V can be generated by the booster.

Both the designed ICs use an SPI interface to implement a bi-directional communication with the external. The experimental setup includes also a Xilinx FPGA Spartan-6 LX45, used as a bridge between the ICs and a PC used to store the recorded data. The FPGA hosts also a digital decimator filter, realized as a third order Cascaded Integrator - Comb (CIC) filter, to downsample the bitstream at the output of the SDM. Fig. 4 and 5 show respectively the layout of the recording and stimulation chip, the first occupies an area of 8.7 mm^2 while the second an area of 17.68 mm^2. The results obtained from measurements confirm the capability of the proposed system of recording neural signals and inject stimuli directly into the PNS.

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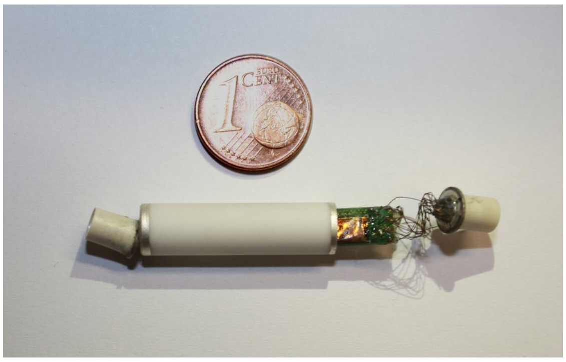

Figure 1: Hermetic Package hosting the ICs

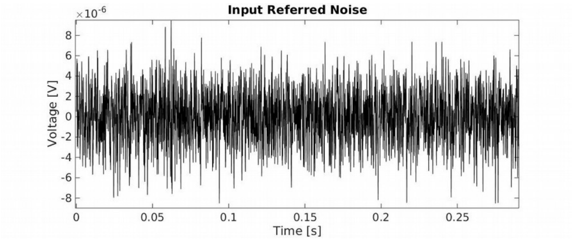

Figure 2: Measured Input Referred Noise

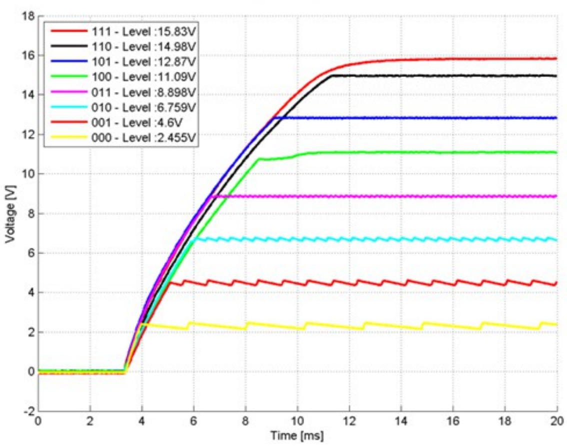

Figure 3: Booster voltage programmability

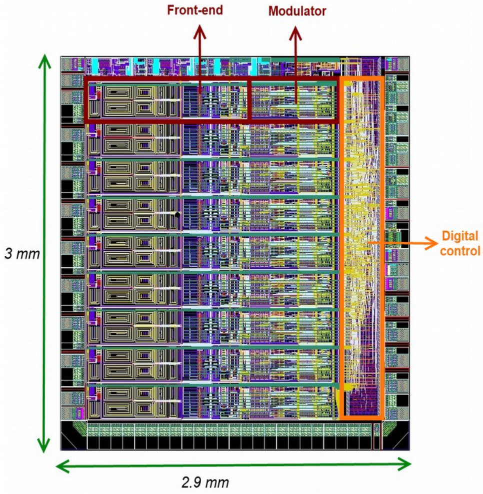

Figure 4: Layout of the recording chip

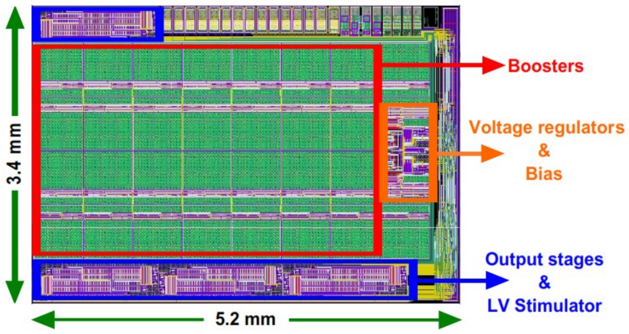

Figure 5: Layout of the stimulation chip

A CMUT Transceiver Front-End with 100-V TX Driver and 1-mW Low-Noise Capacitive Feedback RX Amplifier in BCD-SOI Technology

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An emerging class of portable and handheld ultrasound imaging devices is rapidly expanding and is expected to have a broad market potential. High costs and limited performance, caused by the reduced availability of suitable electronics and by the transducer technology, are the current limiting factors. In this context, the well-known technical characteristics of CMUTs, such as large operation bandwidth and wide operating temperature, together with the cost reduction arising from the adoption of MEMS technology may be leveraged in the development of such kind of devices. In this work, we report on the development of a fully-integrated, low-power analog front-end circuit, specifically designed for 1D CMUT arrays operating in the 1-15 MHz range.

The proposed circuit is shown in Fig. 1. It comprises a high voltage TX driver, the T/R switch and a low noise RX amplifier. Capacitive feedback is exploited in the RX amplifier to achieve better noise-power performance than commonly adopted trans-resistance stages [1]–[4]. A BCD-SOI technology with high-voltage DMOS transistors has been adopted, allowing to deliver up to 100 V transmit pulses. Techniques to minimize loading of the large parasitic capacitances introduced by the high-voltage devices are shown. Moreover, an improved T/R switch is proposed to achieve sufficient isolation of the LNA during transmission and at the same time a low parasitic resistance in on state. A chip microphotograph is shown in Fig. 2. To perform electrical characterization and acoustic measurements in conjunction with a 10-MHz linear array CMUT probe head, the chip prototype has been wire-bonded onto a test board that allows providing the chip with the power supplies and the logic control signals, as well as the CMUT with the bias voltage.

Electrical characterization as well as transmission and pulse-echo measurements with the front-end connected to the CMUT are shown. Results are summarized and compared against recently reported CMUT front-ends in Table 1. The proposed transceiver has the highest TX pulse amplitude, the highest RX dynamic range, and the RX amplifier with the lowest power dissipation. The Noise Figure of Merit, Noise FoM = $N_{in}\sqrt{P_{diss}}$ (being N_{in} the input referred noise and P_{diss} the power dissipation) recently proposed as a benchmark for CMUT amplifiers [1] is more than 2x better than state of the art.

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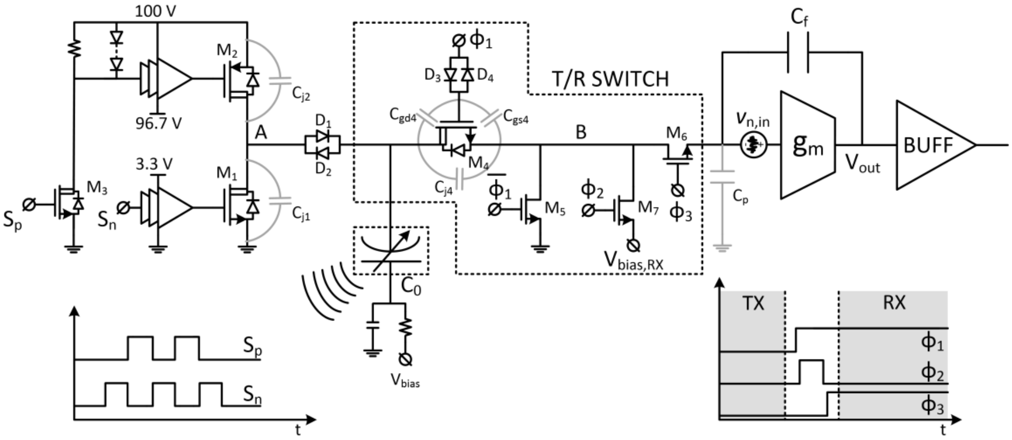

Figure 1: Simplified schematic of the CMUT Front-End.

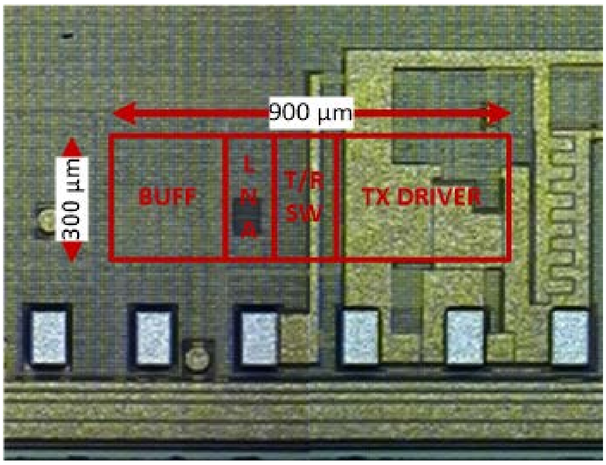

Figure 2: Chip photograph.

	This Work	[1]	[2]	[3]	[4]
Center Frequency [MHz]	10	3	15	2.2	5.1
Bandwidth [MHz]	11	5.2	10	5	6.4
Pulse Amplitude [V]	100	30	n/a	25	25
RX Power Cons. [mW]	1	14.3	6.6	2.4	4
RX Sensitivity [mV/kPa]	72	162	130	414	70
Input Noise [mPa/$\sqrt{\text{Hz}}$]	0.55	0.56	3	0.9	1.8
Dynamic Range [dB]	70	60	42	n/a	n/a
Noise FoM [mPa$\sqrt{\text{mW/Hz}}$]	0.55	2.1	7.7	1.4	3.6

Table 1: Performance summary and comparison.

CMOS I/O protection circuits for automotive applications

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In automotive systems, any I/O and power pin at board level must withstand several voltage stress conditions. A first situation is due to the automotive signal to be detected (for diagnosis or control purposes) which can exhibit voltage peaks up to several hundred volt [1]. A further stress may occur at any pin due to a fault condition at system level leading to a short circuit to either ground or to the car battery rail. A typical approach requires on-board dedicated clamp circuits [2]. In the present abstract a different implementation aiming at maximum integration is presented. The proposed circuits were implemented in a 350-nm HV CMOS technology and characterized over the -40°C to +125°C temperature range.

The first input protection circuit addresses the problem of the detection of a typical automotive signal (i.e. spark coil or fuel injector driving), Fig. 1. An integrated comparator powered by the 5-V board supply performs the required conversion to the digital domain. An interface and protection circuit, Fig. 2, is between the input pad and the comparator. Concurrent ESD and signal over-voltage protection are provided by a GGNMOS stack, featuring a low trigger voltage, and a passive shunt limiter, CLAMP1. A resistive divider (DIV) scales the input signal within the comparator input range. It is worth noticing that this protection is fully passive and only a resistor, R_{EXT}, is required as off-chip component. Stress measurements were carried out with real automotive signals. DC characterization was performed with an input current up to 2mA, corresponding to a peak voltage of 470V with 220-kΩ as off-chip resistor, Fig. 3.

The second proposed circuit is designed to protect the output pin of an analog driver against short circuit to either ground or battery voltage (i.e. 12-18-V) because of a fault condition at system level. The protection circuit must fulfill the following requirements: rail-to-rail signal swing (i.e. 0 to 5-V), to be compatible with an op-amp designed for huge capacitive loads (up to 50-nF) and a minimum number of off-chip devices. The black-box schematic of the driver and the protection circuit is shown in Fig. 4. The opamp is based on the folded cascode architecture with a class-AB rail-to-rail output stage and thin-oxide DMOS output devices. An off-chip power switch is introduced between the 5-V board supply and the power pin of the output stage. When the output pin is shorted to the car battery rail, thus to a higher potential than the opamp supply, a short detector circuit drives the power switch into the open mode. Dedicated clamping circuits have been introduced to avoid any rating condition violations for all devices in the output stage. Measurement results are in good agreement with simulation; in Fig. 5 the transient behavior during the short event is shown. Fig. 6 shows an additional solution for output current sensing and limiting for short circuit events to 0V and 5V. Fig. 7 shows simulated and measured output current in case of short circuit to 0V.

The driver exhibits an area of 0.6mm^2 and a minimum phase margin of 46° with a 50nF load; the open-loop unity-gain bandwidth is 30kHz with a maximum current consumption of 1.9mA.

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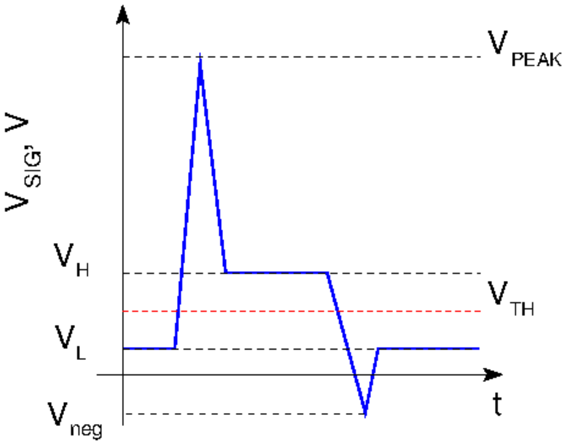

Fig. 1: Spark coil driver output signal (approximation)

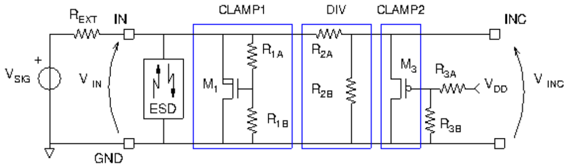

Fig. 2: Proposed protection and interface circuit

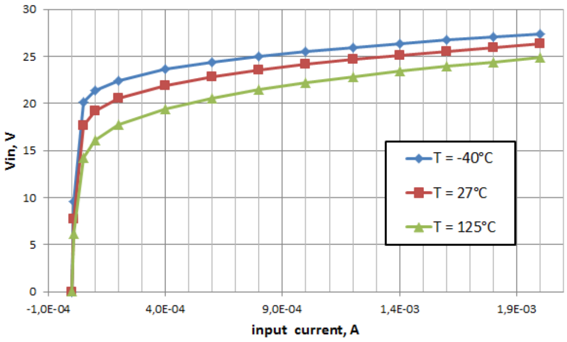

Fig. 3: Pad voltage vs forced input current

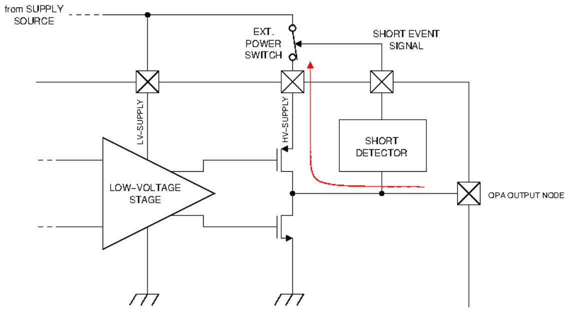

Fig. 4: Circuit solution for withstanding a short event to the car battery supply (18-V)

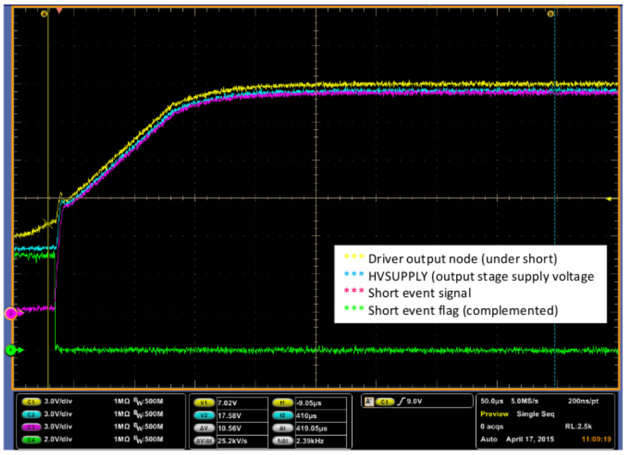

Fig. 5: Short event at the driver output node (transient)

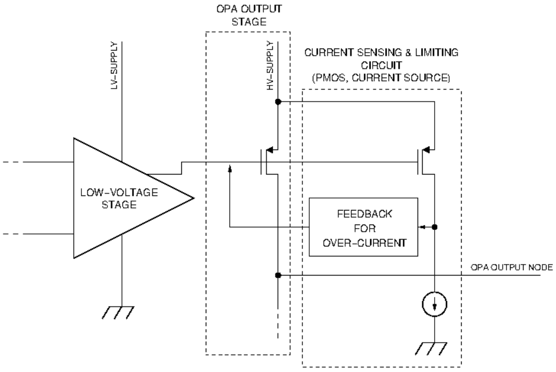

Fig. 6: Proposed circuit for output current sensing and limiting

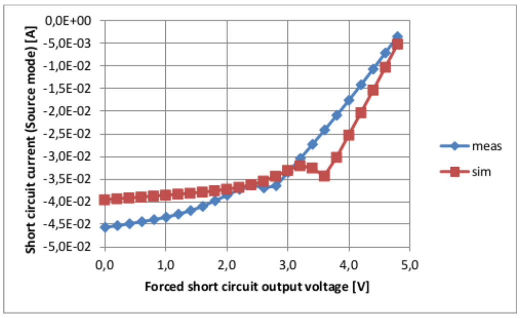

Fig. 7: Short circuit current versus forced output voltage (Source mode)

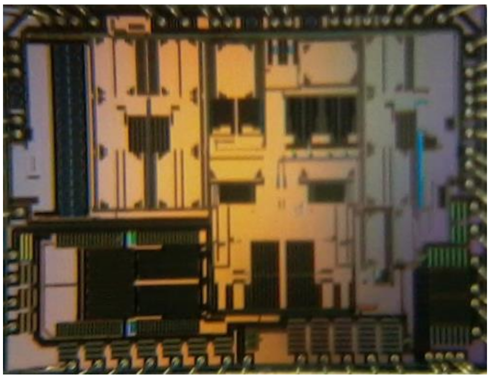

Fig. 8: Die micrograph

Integrated high-performance timing electronics for Time Correlated Single Photon Counting with SPAD Arrays

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The Time Correlated Single Photon Counting (TCSPC) technique is very effective to analyze extremely weak and fast, periodical light signals and then it is increasingly widespread in a large number of fields and in many applications such as fluorescence imaging and laser scanning microscopy[1].

Nowadays, most of the high-performance TCSPC systems are focused on single channel applications[2],[3] and, to obtain a multidimensional system, the use of multiple acquisition chains is necessary, with very high costs and large occupied areas.

However, the development of Single Photon Avalanche Diode (SPAD) arrays is leading to the design of new multichannel TCSPC systems, that can fit the specifics of even more applications. In this domain, the reduction of occupied area and dissipated power are crucial to develop a densely packed timing array. Nevertheless, available TCSPC systems still suffer from a trade-off between number of channels and performance[4],[5]: the higher the number of channels, the poorer the performance on each channel.

In order to overcome this trade-off, we present the design of the integrated electronics necessary to develop photon timing systems featuring either a large number of channels and high performance.

First of all, a circuit capable of directly reading the SPAD avalanche current is of the utmost importance in order to achieve a very high temporal resolution while minimizing the crosstalk. Thus, a fully integrated trans-impedance stage with a gigahertz bandwidth has been designed and fabricated in 0.18 um featuring a time resolution lower than 40ps and negligible crosstalk[6].

Secondly, a fully integrated array of high performance time-to-amplitude converters (TAC) has been designed: starting from the very good results obtained with a first prototype consisting of four independent single channel TACs on the same chip[7], an array of 16 TAC has been designed in 0.35um SiGe technology. The first simulations on the new chip show very high performance on each channel: a time resolution of less than 20 picoseconds on 12.5 ns full scale range, a differential non linearity lower than 1 % peak to peak of the LSB and a conversion frequency of 4MHz.

Finally, an integrated circuit capable of routing the signal coming from the trans-impedance stage towards the TACs has been designed in 0.18 um technology. The routing logic connects the SPAD to one of the TAC converters only if a photon has been detected, thus opening the way to resource sharing: having few TACs in fact allows a larger area and a higher power dissipation for the single converter which contributes to achieve very high performance in terms of time resolution and linearity.

In conclusion, three fully integrated circuits have been designed: a pick-up circuit to read the SPAD current, a routing logic to feed the electrical signal coming from the SPAD to the time measurement blocks and an array of TACs to properly measure the time interval. The development of these building blocks can lead to the design of innovative architectures for TCSPC measurement, featuring both a large number of channels and very high performances on each channel.

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Pollution gas sensing devices composed by LDH nanostructures connected to wearable ultra-flexible readout circuit based on polysilicon

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The international governance has set air quality standards for six common air pollutants [1, 2] carbon monoxide (CO), ozone (O_3), lead (Pb), nitrogen dioxide (NO_2), particulate matter (PM), sulfur dioxide (SO_2). These pollutants can provoke severe damages for human health and for the environment in general. Today, measurements for urban pollution are carried out by big environmental monitoring stations across the country. An important development could be given by massive and distributed monitoring of air quality, exploiting the human presence itself. This may be achieved by providing a monitoring wearable device. Wearable electronics and pervasive ambient computing are two scenarios where largely distributed flexible sensors networks are expected to be heavily used [3]. The growing demand for sharing large stream of data among groups of people in different places at different times is now pushing researchers and scholars toward the creation of individual smart sensors networks. In such a network, each person constitutes a node of the web or, on the other hand, toward the development of smart sensing infrastructures, where some information can be concentrated in a place and can be exchanged simply passing through them. In this work resistive sensors based on Layered Double Hydroxides (LDHs) have been fabricated and tested, connecting these devices to readout electronics based on polysilicon embedded on flexible substrate. LDH material was chosen since it is characterized by a large surface to volume ratio and it shows a strong ability to adsorb molecules of any kind. For the first test, several sensors were grown on an interdigitated structure on a rigid holder but in future the LDHs can be fabricated on flexible substrates [4]. In figure 1a and 1b a sensor and a SEM image of the LDH material are respectively shown. The sensors, placed in a gas-measuring chamber, have been exposed to several concentrations of NO_2 diluted in wet air to obtain a constant flux of 200 sccm at room temperature and then cleaned in wet air. An example of sensor response at NO_2 impulse is shown in figure 2. Elementary building blocks in polysilicon n-MOS thin film transistors (TFTs) [5] have been used to design the flexible readout circuit. The polysilicon electronics presented here is based on n-MOS technology to merely simplify the manufacturing process and reduce the fabrication costs. The TFTs exhibit low leakage current (< 1pA), on/off ratio of 10^5, mobility of 30 cm^2/Vs, threshold voltages of 5 V, low kink effect and subthreshold slope of 400 mV/dec as shown in fig. 3a-b. The final circuit will be fabricated by using high compact configuration, manufacturing at least one amplification stage and a buffer for decoupling impedance and taking into account sensor thermal balance (see fig. 4). In conclusion, the optimization of a device based on LDH material and polysilicon flexible electronics can provide a suitable solution for air quality monitoring, exploiting the wearability and the potential high sensitivity of these devices.

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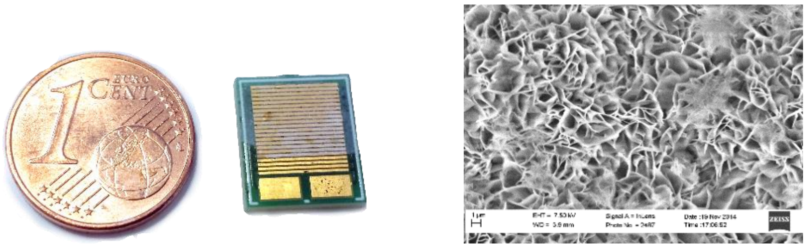

Figure 1 a) Interdigitated fingers covered by LDH structure. b) SEM image of the LDH structure growth on the interdigitated fingers.

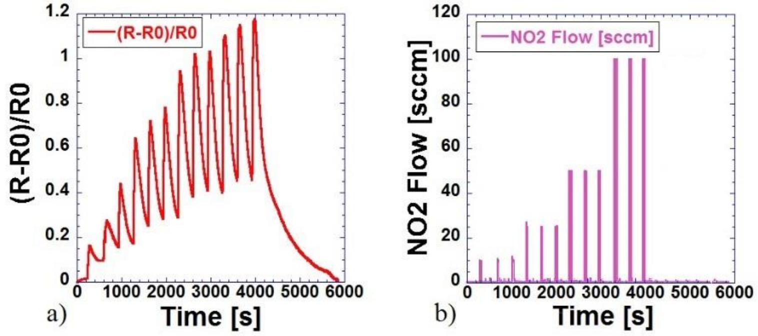

Figure 2 An example of sensor response at NO_2 impulse, a) normalized response of the LDH sensor, b) the respective increasing flows of NO_2

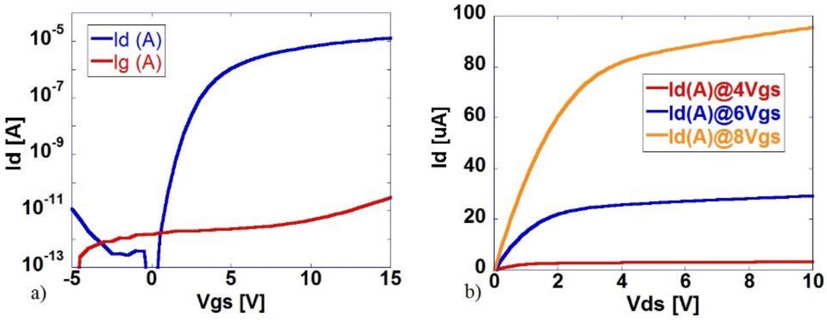

Figure 3 The typical transfer characteristic of polysilicon TFT fabricated on polyimide ultra-flexible substrate; in red the leakage current through the gate (a); the output characteristics from increasing gate voltages (b).

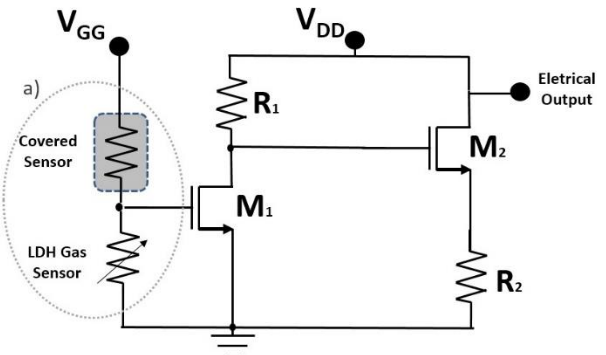

Figure 4 The readout circuit, a) detail: the dummy-sensor is encapsulated so as not to be exposed to the gas and allow the thermal balance.

A neuromorphic synapse with resistive-switching devices capable of on-line pattern learning

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Neuromorphic computing is raising huge interest for low-power, reconfigurable, massively-parallel bio-mimetic applications, such as on-line learning, pattern recognition and robotics [1]. To match the required ultra-high connectivity (~10^4 connections per neuron in the human brain), small-area and low-power synapses are needed. To this purpose, resistive switching memory (RRAM) based on metal oxides are ideal candidate for such application [1]. Here we present a 2-transistor/1-resistor (2T1R) synapse capable of communication and conductance update based on the spike-timing dependent plasticity (STDP) protocol [2], discussing the architecture, operation and capability in terms of learning and recognition of visual patterns.

Fig. 1a shows the circuit layout of the 2T1R synapse, where the top electrode (TE) and the control gate (CG), namely the gate of the first transistor, are connected to the pre-synaptic neuron (PRE), while the fire gate (FG), namely the gate of the second transistor, is controlled by the post-synaptic neuron (POST). The resistance consists of a RRAM device with tunable conductance. Communication between the 2 neurons is activated by spike pulses applied to the CG and the TE as shown in Fig. 1b. The resulting currents are integrated by the POST, which eventually fires as the internal (membrane) potential exceeds a given threshold (Fig. 1c) [2]. The fire pulse excites the FG, which interacts with the PRE spike differently depending on the time delay Δt between fire and spike, according to the STDP protocol in Fig. 2. For $\Delta t > 0$, namely if the PRE spike precedes the fire (a), the FG pulse overlaps with the positive part of the TE pulse, thus inducing set transition (conductance increase) in the RRAM which corresponds to long term potentiation (LTP) of the synapse. For $\Delta t < 0$, namely if the PRE spike follows the fire (a), the FG pulse overlaps with the negative part of the TE pulse, thus inducing reset transition (conductance decrease) in the RRAM which corresponds to long term depression (LTD). Fig. 3 shows the cumulative distributions of resistance R after LTP for variable $\Delta t > 0$ (a) and the corresponding median values as a function of Δt (b). The RRAM in the synapse was a HfO_x-based device which was always prepared in the high resistance state (HRS) before STDP. Fig. 4 shows the cumulative distributions of resistance R after LTD for variable $\Delta t < 0$ (a) and the corresponding median values as a function of Δt (b), where the RRAM was always prepared in the low-resistance state (LRS) before STDP. Fig. 5 shows more STDP characteristics for variable HRS (a) and variable LRS (b), indicating LTP and LTD for $\Delta t > 0$ and $\Delta t < 0$, respectively. Data show controllable LTP and LTD, thus supporting the STDP functionality of our synapse scheme.

To assess pattern learning and recognition of our 2T1R synapse, we simulated the perceptron in Fig. 6, namely a 2-layer neural circuit with N PRE and M POST. The 1st layer mimics a retina delivering the visual pattern interlaced with random noise to the 2nd layer. Fig. 7a shows the original pattern and the synaptic weights at increasing epoch (PRE-spike event) for the simulation results for N = 64 and M = 1. The simplified STDP characteristic in Fig. 7b was adopted. Fig. 7c shows the evolution of weights of the 64 synapses over 1000 epochs. The neuromorphic circuit shows LTP of pattern synapses and LTD of all other synapses, thus confirming the ability to efficiently learn visual patterns in the RRAM-based 2T1R synapses.

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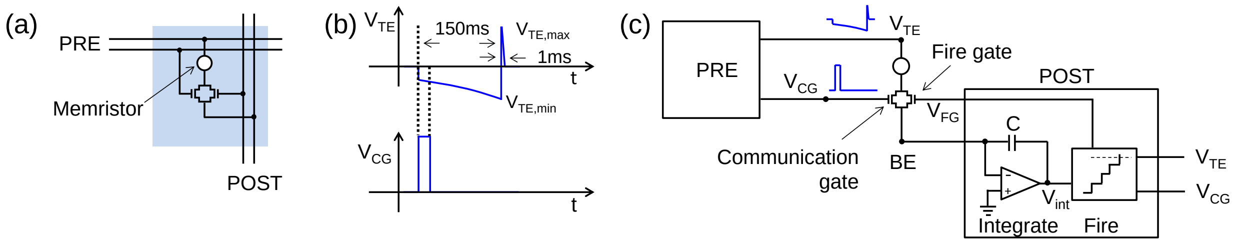


Fig. 1 Conceptual demonstration of a 2T1R synapse (a). (b) shows the applied pulses during communication, while (c) shows the complete pre-synapse-post architecture.

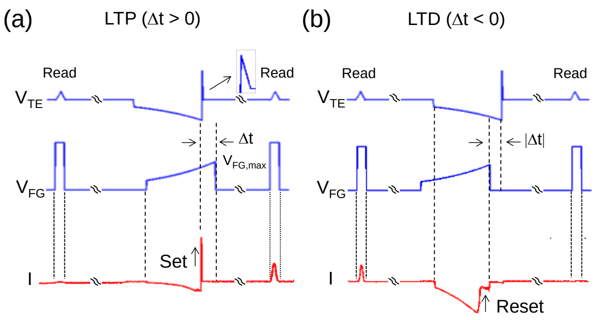


Fig. 2 Applied pulses to the top electrode and fire gate during LTP (a) and LTD (b).

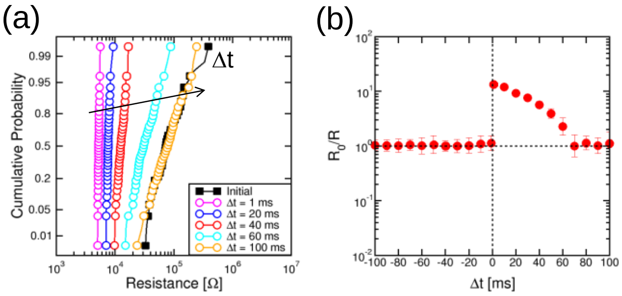


Fig. 3 Measured resistance distributions for LTP (a) and corresponding median values (b).

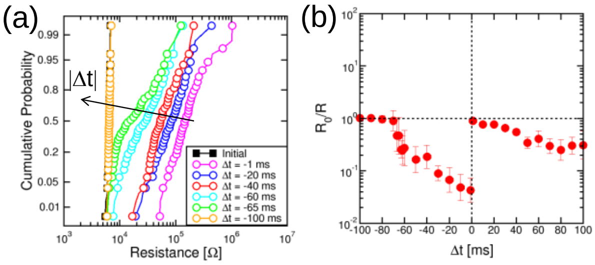


Fig. 4 Measured resistance distributions for LTD (a) and corresponding median values (b).

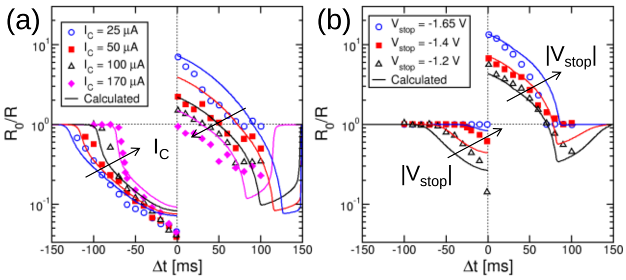
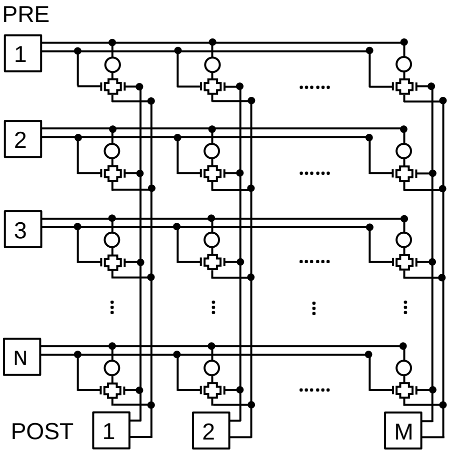


Fig. 5 Measured and calculated STDP curves starting from different LRS (a). (b) reports measured and calculated STDP curves for different initial LRS states.



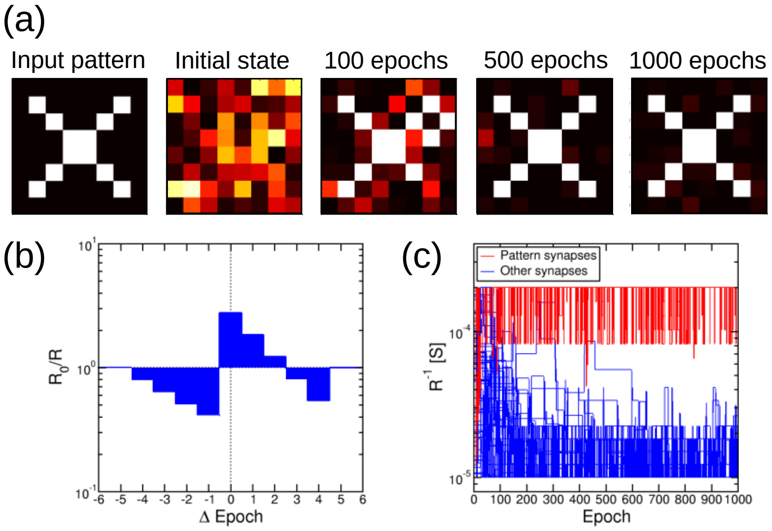


Fig. 6 Architectural scheme adopted for a 2-layer pattern learning simulation.

Fig. 7 Simulations. (a) shows the input pattern together with the time evolution of the synapse weights, obtained with the simplified STDP of (b). (c) shows the 64 synapses conductance evolution.

Electrostatic interactions in nanoscale oxide stacks

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The CMOS technology scaling is enhancing single-charge related phenomena such as BTI and RTN, which represent a major reliability concern for nanoscale devices (e.g. FinFETs, RRAM). Here we show that the electrostatic interactions among charge carriers trapped at defect sites in nanoscale oxide stacks may be responsible for RTN. The RTN is investigated in TiN/Ti/HfO_x/TiN RRAMs in High Resistive State (HRS) [1]. RTN traces recorded at different temperatures and voltages are analyzed using the FHMM [2], which allows decomposing the multi-level RTN signal into a superposition of two-level fluctuations, each associated with the way an individual defect interacts with the electric field. Charge transport and RTN are simulated using MDLab, considering the multi-phonon trap-assisted tunneling (MP-TAT) [3] and the 3D potential map including the trapped charge. The HRS current is due to the electron MP-TAT [3] at Vo^+ (O vacancy) defects in the re-oxidized tip of the conductive filament (barrier). RTN is considered to be caused by the (de-)activation of Vo^+ defects assisting charge transport [4]. This is confirmed by simulations of ΔI distributions, performed by calculating the current contribution driven by individual Vo^+ defects distributed within the barrier, Fig. 1. A uniform distribution of Vo^+ defects ($N_T=2\cdot10^{21}$ cm^{-3}) allows reproducing the ΔI distributions measured during cycling in different conditions. The thickness of the barrier is extracted from I-V curves through the compact model in [5]. The simulations of the RTN ΔI statistics allow calculating the distributions of electron capture/emission times at Vo^+ defects, which lie in the sub-ns regime, Fig. 2, and are orders of magnitude smaller than those extracted from RTN measurements, Fig. 2. This points to a different defect species involved in the (de-)activation of the Vo^+ defects. Here we consider a defect of different nature located close to the Vo^+ (assisting the MP-TAT current), interacting with the Vo^+ via electrostatics. The potential perturbation generated by charge trapped at a "slow" defect (located in the surroundings of the fast Vo^+ defect assisting the HRS current) deeply affects the alignment between the electrons and the ground state of the fast Vo^+ trap, Fig. 3. This alters the MP-TAT current, resulting in RTN. To quantify the amount of the interaction, we simulated the effect of a negative charge (i.e. electron trapped at a "slow" neutral defect) on the current driven by a single Vo^+ defect as a function of their distance, Fig. 3. I-V simulations show that the current is reduced at short distances (<1nm) due to strong Coulomb interaction. Hence, the charge capture/emission into/from "slow" defects may inhibit the electron MP-TAT through a close Vo^+ defect causing the observed RTN, Fig. 4. This is confirmed by Kinetic Monte-Carlo simulations of charge transport at Vo^+ defects including charge trapping at "slow" defects in their proximity, Figs. 5-6. This model is used to achieve a physical characterization of RTN. Fig. 7 shows RTN traces recorded at different voltages. ΔI and RTN τ_c and τ_e were extracted for each fluctuation. The ΔI can be regarded, in first approximation (i.e. strong Coulomb interaction), as the current driven by a Vo^+ defect when the close "slow" defect is empty. Thus, the position and energy of the Vo^+ defect can be extracted by simulating ΔI as the current driven by the Vo^+ defect at different voltages, Fig. 8. RTN τ_c and τ_e in different conditions are consistently simulated considering the MP-TAT through a "slow" defect, Fig. 9.

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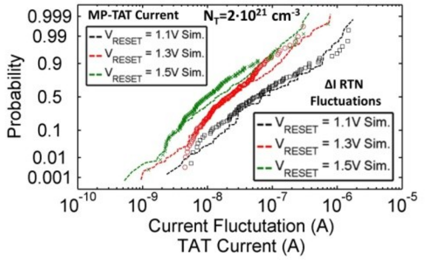

Fig. 1 – Simulated MP-TAT current at Vo^+ (lines) and experimental ΔI RTN (symbols) statistics over cycling for different devices. ΔI corresponds, in first approximation, to the current contribution of an individual Vo^+ defect in the active state.

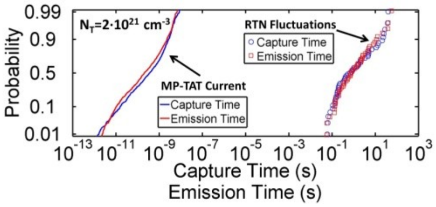

Fig. 2 – Simulated (lines) capture and emission times for Vo^+defects (MP-TAT current) and experimental (symbols) RTN capture and emission times. Typical RTN and charge transport dwell times are orders of magnitude apart from each other.

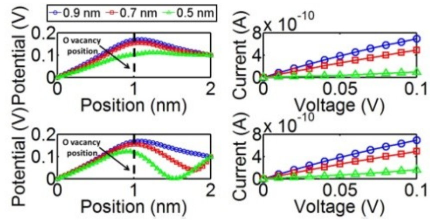

Fig. 3 – Simulated potential profiles along the device thickness (left) and I-V curves (right) for a single Vo^+ (the position of which is fixed) and a negative charge (the position of which changes) as a function of their distance in the planar (top) and vertical (bottom) directions. The applied bias is 0.1V.

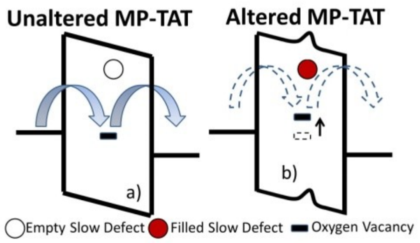

Fig. 4 – Schematic representation of the RTN mechanism. (a) The MP-TAT transport via a fast Vo^+defect. (b) The electron capture by the slow defect significantly affects the energy alignment between the electrons and the ground state of the fast Vo^+defect, suppressing the current at the $Vo^+$and causing RTN.

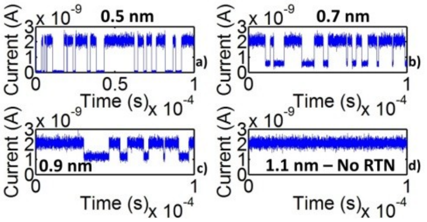

Fig. 5 – Kinetic Monte-Carlo traces of RTN for different distances (a-d) of one slow defect from a single Vo^+. The superimposed white noise due to the average effect of the fast Vo^+capture and emission processes is also simulated.

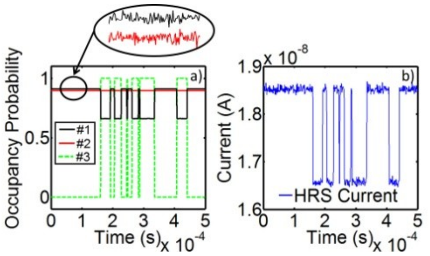

Fig. 6 – (a) Kinetic Monte-Carlo simulations of two Vo^+ (#1 and #2) and a slow defect (#3), close to the Vo^+ (#1). The occupancy of the Vo^+ #2 is not perturbed. The occupancy of the Vo^+ #1 changes over time due to the coulomb interaction with #3. The resulting overall current is show in (b).

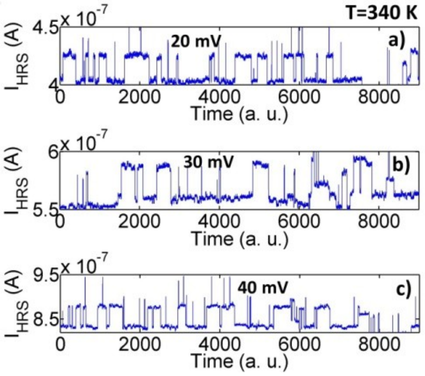

Fig. 7 – Experimental RTN traces recorded at different voltages on a device, without altering its state.

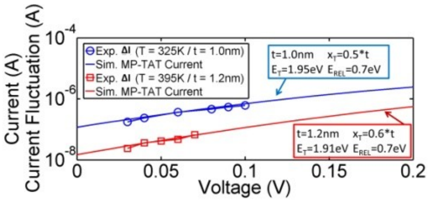

Fig. 8 – Experimental ΔI (symbols) from different devices and conditions (temperature and voltage). Simulated MP-TAT currents (lines) are also reported. The properties of the considered Vo^+ defects are highlighted.

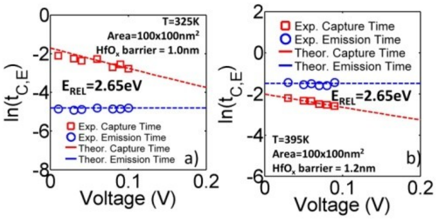

Fig. 9 – Simulated (lines) and experimental (symbols) RTN capture and emission times for the two devices in Fig. 8. Simulations consider the MP-TAT process at an additional slow defect.

Fabrication and characterization of Micrometer-scale ZnO memristors

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Memristors are an interesting class of resistive random access memory (RRAM) based on the electrical switching of metal oxide film resistivity [1]. They are considered the next generation of non volatile memories. The device structure is simply an oxide layer sandwiched between two metal electrodes. The switching behaviour is dependent both on the oxide material and the choice of metal electrodes. For this reason switching characteristics of many metal oxide films (e.g. TiO_2, NiO, TaO_2, HfO_2) and metal contacts have been studied [1]. ZnO has attracted much attention as an oxide material for memristor application, due to its abundance in nature, which means low cost, and compatibility to CMOS technology [2] in terms of process integration and device scalability down to nanometric sizes.

In this work we report on the fabrication and electrical characterization of microscale ZnO memristors. The structure of each device is shown in Fig. 1. The first step of the memristor fabrication consisted of the deposition of a 40 nm-thick ZnO thin film by pulsed laser deposition (PLD) on fluorine-tin-oxide (FTO)/glass substrate. Afterwards, Al pads of different sizes ranging from 100 × 100 to 300 × 300 μm^2 and 150 nm thickness were defined by direct laser-writing microlithography and subsequent lift-off. All devices were electrically characterised at room temperature by performing two-probe I–V measurements by means of a custom developed electronic circuit. Fig. 2 shows the typical I–V curves of two memristors with 100 × 100 and 300 × 300 μm^2 active areas. The voltage was swept in the range –3 to 3 V, by following the cycle described by the arrows (1→5). Fig. 3 displays the dependence of the high resistance state (HRS) and low resistance state (LRS) at 1.4 V upon the device size. LRS is independent on the device area, suggesting that the ON-state of the device is dominated by a local, filamentary phenomenon. HRS instead increases as the device area is reduced, and the best R_{OFF}/R_{ON} ratio (21.5) is obtained for the smallest device (100 × 100 μm^2). Moreover, LRS looks very stable, with very small fluctuations compared to those of HRS. Fig. 2 shows also that each ZnO memristor exhibits a different reset voltage: in particular the 300 × 300 μm^2 device, having a larger active area, switches to the HRS for a higher voltage. This is due to the fact that larger devices have larger quantity of filaments responsible of conduction. This can also be seen in Fig. 3, where the larger devices have a lower HRS. LRS instead does not depend on the device size, since in the ON-state the number of parallel conducting filaments due to the motion of oxygen vacancies is so large that each device resistance is well defined regardless of the device active area.

In conclusion, the results show that HRS increases with decreasing of devices' size. This suggests that further work must be addressed toward nanoscale ZnO memristors, which are expected to give a larger R_{OFF}/R_{ON} ratio, much more suitable for memory applications.

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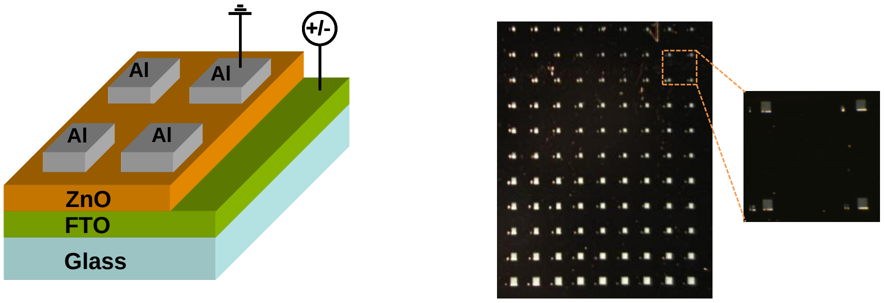

Figure 1: Sketch of the fabricated devices and electrical measurements arrangement (left). The measurements were performed by applying a digital voltage ramp with steps of 50 mV to the FTO bottom contact, with the Al top contact grounded. Optical microscope image of the fabricated memristors (right). The inset shows a magnified image of the $100 \times 100\ \mu m^2$ devices.

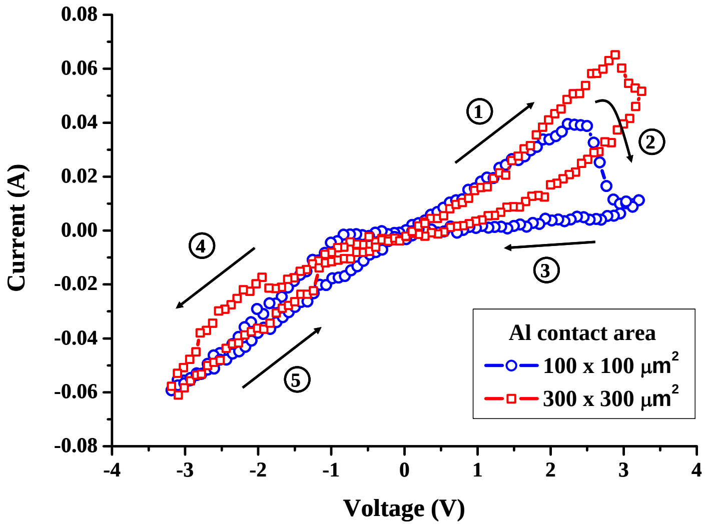

Figure 2: Typical I–V characteristics (after 10 cycles) of Al/ZnO/FTO memristors for two different Al contacts size. A forming process was first performed by sweeping the voltage in the range 0–4 V. The arrows show the direction of the hysteresis cycle: point 2 marks the RESET process (switching from the LRS to the HRS), instead point 4 indicates occurring of a SET process (switching from the HRS to the LRS). All devices fabricated exhibit a typical bipolar nature since they can only be switched to the high resistance state (HRS) by the positive voltage.

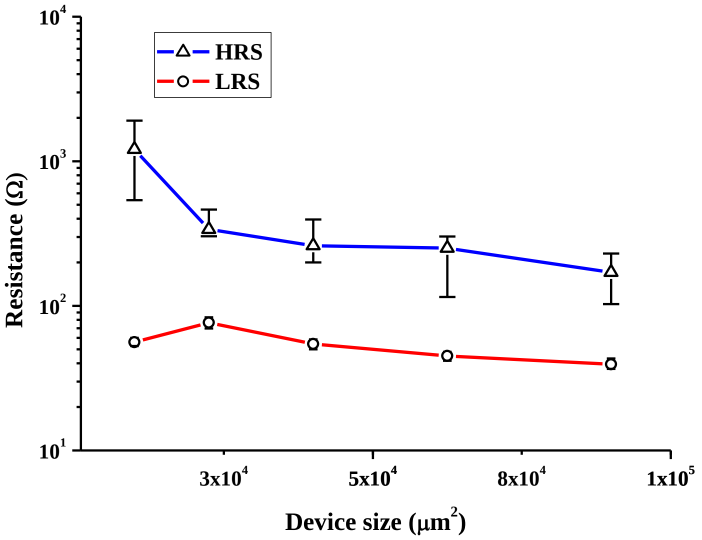

Figure 3: Resistance in the ON (LRS) and OFF (HRS) state against device size for the Al/ZnO/FTO memristors.

Including RDF in surface potential-based compact MOSFET models

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For deeply scaled technologies, the modeling of random process variations on the electrical device performances (the so-called *variability analysis*) has become of primary importance in the design of both analog and digital MOSFET-based circuits [1]. Among the various possible degrees of variability [2], we focus here on the treatment of device level variations only.

Among the possible causes for device-level variation (namely, metal gate work function variations, process variation effects, and random dopant fluctuations), a major role in influencing the variability of electrical performances is played by the intrinsic granularity of doping inside the device channel [1]. From the standpoint of modeling, up to now the effect of random, space-dependent dopant fluctuations has been mainly analyzed through physics-based, numerical 2D or 3D simulations. Representative approaches are the drift-diffusion transport model (including, in some cases, quantum corrections based on the density gradient method) [1][3][4] or more complete, higher-order carrier transport models [5], which is more accurate in describing deeply scaled devices. From the numerical standpoint, variability analysis is especially challenging while Monte Carlo-like simulations with varying doping values randomly distributed in the device according to a Poisson distribution, turn out to be extremely time consuming. Recently, linearized approaches to variability analysis, like the Green’s function approach [4] implemented into the Sentaurus TCAD simulator, have been proposed in order to overcome the limitations of the Monte Carlo approach and more efficiently assess the device variability. Literature results concerning the analysis of threshold voltage variability versus dopant fluctuations suggest that a linear perturbation theory may be accurate enough in practical situations, besides being, at any rate, a first modeling step [6].

We propose here a general methodology to include the effect of device-level position-dependent random doping fluctuations (RDFs) into compact MOSFET models through a Green’s Function approach, akin to the physical device variational analysis. In particular, such a methodology is developed within the MOS analytical models based on the charge-sheet approximation, with particular emphasis to the so-called surface potential models [7]. The effect of the technological variations of local doping is directly estimated in terms of the drain current fluctuations with respect to the value obtained with nominal doping, rather than from the variations induced in the threshold voltage only. Furthermore, the methodology is used also to assess the quasi-static small-signal device parameter variations.

The modeling strategy, detailed in [8], has been applied to the PSP compact model that, both for the part concerning the DC analysis and for the part concerning the variational approach based on the Green’s functions, , has been implemented into the Agilent ADS circuit simulator by means of a Verilog-A code. The PSP model has been first carefully calibrated against numerical TCAD simulations, including the variation part (i.e. Green’s Functions, see Fig. 1).

We show results for a 180 nm gate n-channel MOSFET (substrate doping $N_A=1.5\times10^{18}$ cm^{-3}). The threshold voltage is around 0.5 V. Such a gate length is compatible with up-to-date analog CMOS applications. In order to assess the validity of the Green’s function approach for small-signal analysis, we performed preliminary simulation of three main small-signal parameters, that is, the device transconductance g_m, the device output conductance g_{DS}, and the gate-source capacitance C_{GS}. For this analysis, we have considered only a deterministic variation of 1% of the nominal doping concentration. We compare results from the Green's function linearized approach to an incremental analysis made repeating two times (with nominal doping and doping increased by 1%) the full PSP simulation. Figure 1 shows an example of the variation of the MOS transconductance and MOS output conductance as a function of the gate voltage. The agreement of the linearized model and the incremental approach is extremely good. The same kind of agreement can also be observed for the gate capacitance as a function of V_{GS}, as shown in Figure 2.

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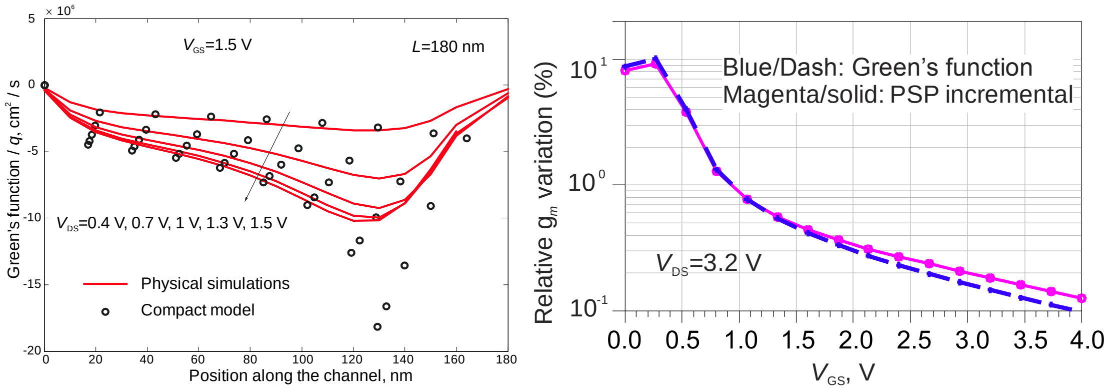

Figura 1. Left: validation of the Green's functions in the PSP compact model vs. the TCAD simulations. Right: comparison of the g_m variations resulting from 1% doping variation of the nominal value.

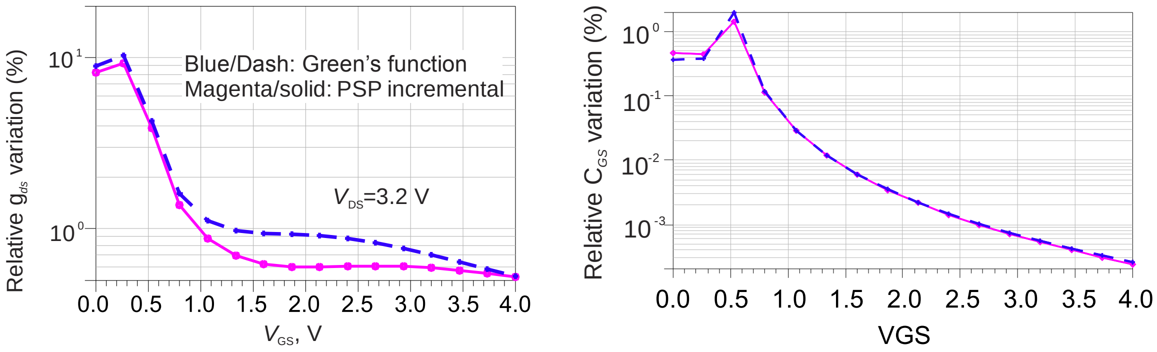

Figura 2: Comparison of the g_{DS} and C_{GS} variations resulting from 1% doping variation .

Low-voltage high-performance III-V semiconductor MOSFETs for advanced CMOS nodes: impact of strain and interface traps

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INTRODUCTION: Integration of III-V compound semiconductors onto Silicon has recently made remarkable progress. In fact, III-V semiconductors offer higher electron velocity [1] than strained Silicon (sSi) and hold the promise of a higher ON current at the same OFF current (Fig. 1). Consequently, the supply voltage V_{DD} can be reduced, with remarkable savings in dynamic power. These characteristics make III-V devices good candidates for fulfilling the ITRS requirements for next generation MOSFETs (Table 1) [2]. III-V-MOSFETs pose new problems due to the still poor quality of the channel / dielectric interface, where a large trap density can harm the device's performance. In the following, we describe the impact of these traps on the device characteristics and the interplay with the strain mobility booster applied to the channel.

MODEL FOR TRAPS: Traps capture and release electrons, resulting in a net negative charge lying in a thin sheet at the channel / dielectric interface. A fraction of the V_{GS} drops across the interface; consequently, the free inversion charge in the channel cannot increase too much. The phenomenon is called Fermi Level Pinning and limits the free inversion carrier density (N_{INV}) at high V_{GS} (Fig. 2) [3]. Figure 3 shows the interface trap density per unit of area and energy (D_{it}) necessary to reproduce the experimental Fermi-level-pinning for unstrained III-V channels from [4]. This D_{it} is large in the conduction band. The trap states are easily populated by electrons because the low effective mass of III-V materials makes them remarkably degenerate. If a 0.46% biaxial tensile strain is added to the channel [4] the conduction band energy shifts by 33 meV (Fig. 4) [3,5]. If we embrace the reasonable assumption that the D_{it} referred to the vacuum level does not change, then the shift of the conduction band entails an identical horizontal shift of the D_{it} (E) with respect to the unstrained case (Fig. 3, blue curve). This reduction of the D_{it} entails that a higher N_{INV} can be reached before Fermi level pinning occurs (Fig. 2, blue curve).

RESULTS: MOBILITY: Both traps and strain affect the effective channel mobility. In fact, the trapped charge affects the electrostatics (via the Poisson equation), and the transport (trapped charges act as Coulomb scattering centres). Strain modifies the band structure of the semiconductor but also the trapped charge since, as discussed above, it lowers the D_{it}. Figure 4 compares the extracted [4] effective mobility with accurate Multi-Subband Monte Carlo simulations [5] based on the coupled solution of the Poisson, Schrödinger and Boltzmann transport equations [6]. The model reproduces reasonably well the trends seen in the experiments, and thus it can be used to predict the on-current of short channel transistors.

RESULTS: ON-CURRENT IN SHORT CHANNEL DEVICES: We consider the aggressively scaled devices as in Fig. 6. Fig. 7 shows that strain helps improving the ON current only when traps are considered. This is because in III-V MOSFETs the strain induced subband modulation is modest, so that the main benefit of biaxial strain comes from a reduced D_{it} [5].

Acknowledgements: This work received funding by the European Community's FP7/2007-2013, grant agreement III-V-MOS Project no. 619326via the IUNET consortium.

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	HP	LOP	LSTP	III-V/Ge
Speed (I/CV)	1	0.5	0.25	1.5
Dynamic Power (CV^2)	1	0.6	1	0.6
Static Power I_{OFF}	1	$5x10^{-2}$	$1x10^{-4}$	1

Table 1: ITRS scaling scenario. HO, LOPD and LSTP are silicon MOSFETs. III-V MOSFETs (last column) should be 1.5 times faster than HP silicon ones, having the same I_{OFF} and working lower V_{DD} to reduce by a factor of 0.6 the dynamic power.

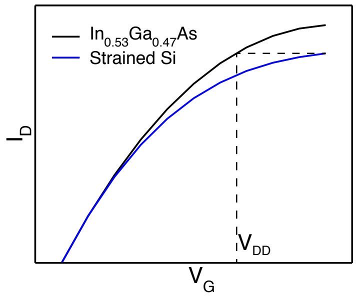


Figure 1: Qualitative representation of the I_{ON} improvement achieved by high mobility III-V compound semiconductor MOSFETs.

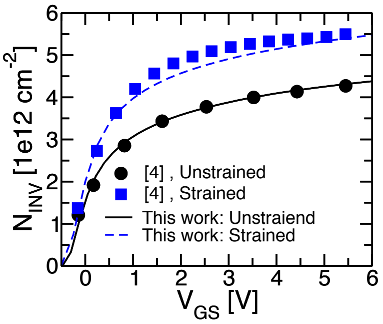


Figure 2: Simulated inversion electron density compared with experiments from [4] for a III-V MOSFETs with 4 nm Al_2O_3 and a $In_{0.53}Ga_{0.47}As$ channel.

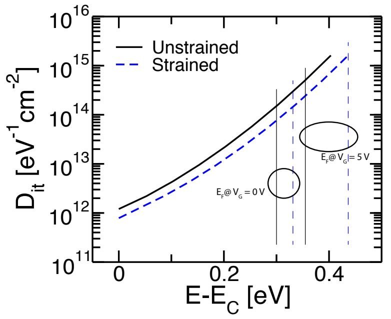


Figure 3: D_{it} used to fit experimental NINV in Fig. 2. The blue-dashed line is the shift of the unstrained curve by 33 mV, equal to the CB shift induced by 0.46% biaxial strain, see Fig.4.

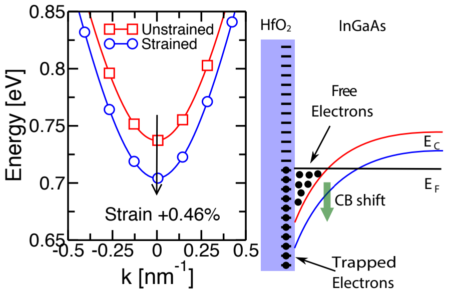


Figure 4: Conduction band lowering due to a 0.46% biaxial tensile strain [4]. Note that the D_{it} profile stays constant with respect to the vacuum level.

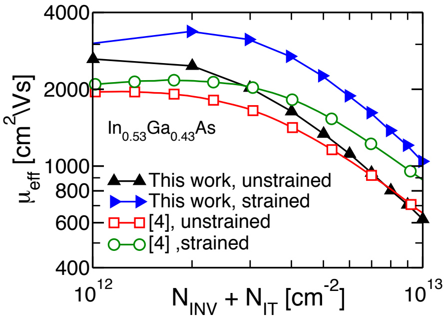
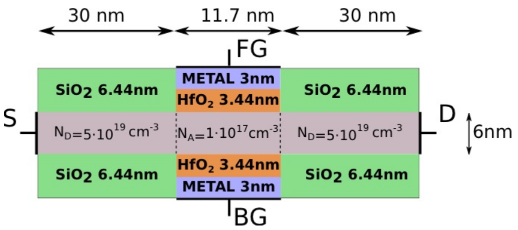


Figure 5: Simulated and experimental mobility in unstrained and biaxially strained (0.46% tensile) long channel $In_{0.53}Ga_{0.47}As$ MOSFETs [4]. Simulations include the effect of interface traps as Coulomb scattering centres (profiles from Fig. 3).



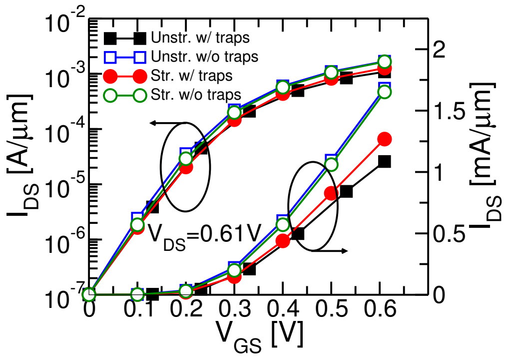


Figure 6: Sketch of the device simulated in this work and designed according to the ITRS roadmap for III-V transistors: L_G=11.7 nm, EOT=0.62 nm, film thickness 6 nm.

Figure 7: I_{DS} vs. V_{GS} for the device in Fig. 6 considering strained and unstrained (biaxial strain 0.46%) $In_{0.53}Ga_{0.47}As$ channel. D_{it} profiles are from Fig. 3 and are applied to both interfaces of the double gate structure.

Micro-for-Nano: a synergy between nanomaterial and CMOS electronics for sensing applications

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During the last years, nanomaterials have been used not only for standard sensor applications, but also to conceive nanodevices (also called *nanosensors*) with increased sensitivity and accuracy, since they are composed by a single nanostructured element. Nanowires (NWs), bridging molecules or nanoparticles, are considered the basis for a new generation of sensors able to interact with gases, molecules (e.g., DNA molecules) or other bio-substances at nanoscale [1]. The fabrication process of a nanosensor (i.e., the integration of a single functonalized nanomaterial with metal electrodes) is usually complex and implies high costly instruments. A low-cost technique is the Dielectrophoresis (DEP), i.e. an electrically controlled deposition of nanomaterials suspended in liquid solution [2].

Fundamentally, the fabricated nanodevice behaves as a passive sensor that changes its electrical properties (e.g., capacitance or resistance) when exposed to sensed quantity. The signal of semiconductor NWs is usually a current in the pA − μA range and the coupling noise, due to long interconnections between nanodevice and electronics, can easily affect the whole sensitivity of the measurement system. Hence, a new approach both for the nanosensor fabrication and for the read-out is strictly required to improve measurement accuracy. The electronic interface needs to be placed as close as possible to the nanodevice to avoid interferences at the interconnections. The best way for reducing coupling noise is to integrate the chosen nanomaterial onto the silicon chip surface and to use top electrodes and metal layers of the CMOS technology for interconnecting the nanosensor with the designed CMOS Read-Out Circuit (ROC). Fig. 1 and Fig. 2 report post-processing on CMOS chip needed to integrate NWs onto CMOS chip exploiting DEP technique.

Anyway, a single nanosensor is not sufficient to produce reliable results because of the large process variation in nanodevice fabrication. Thus, an array of nanosensors is strongly suggested since an average measurement can compensate the defects in single nanodevice fabrication. To enable a high-density nanosensor array on CMOS chip (e.g., 100 nanosensors / mm^2) and preserving high-accuracy and real-time measurements, each nanosensor should be connected to a dedicated small size and ultra-low power ROC able to detect 1% of resistance (or capacitance) variation within the whole measurement range (e.g., 100kΩ – 10GΩ for semiconductor NWs) [3]. Moreover, the read-out system has to overcome flicker-noise effects during DC or low-frequency measurements. ROCs based on oscillators with digital control inputs and 1-bit quasi-digital (e.g., PWM or frequency modulated) output signal can also reduce the complexity of the array management and enable the direct interface with a wireless transmission of data through an ultra-low power impulse-radio transceiver (IR-UWB) [4].

The final aim is to conceive a flexible CMOS platform that implements a Micro-for-Nano (M4N) system where nanosensors and microelectronics coexist on the same device (see Fig. 3). Following this approach, the M4N chip can be used for creating an integrated multi-sensors system for gas detection, a bio-sensor for laboratory analysis or a multi-sensor device for robotics, depending on the functionality of the nano-layer deposited on top (see Fig. 4).

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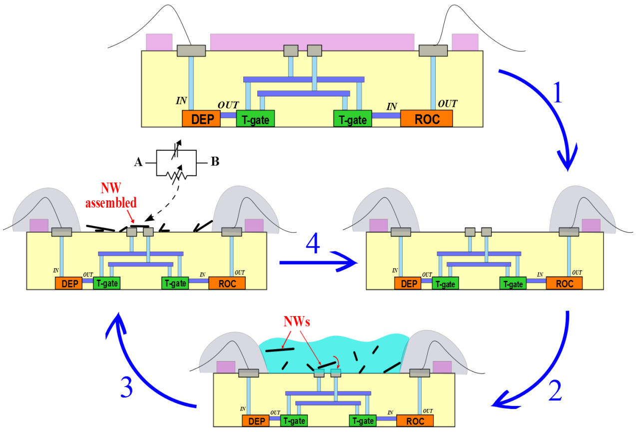

Fig. 1 : Process for NW integration on M4N chip

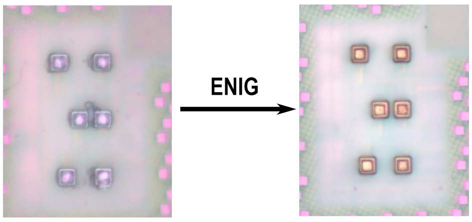

Fig. 2 : Ultra-low cost post-processing on CMOS chip for gold-metallization of top electrodes based on Electroless Nickel and Immersion Gold technique.

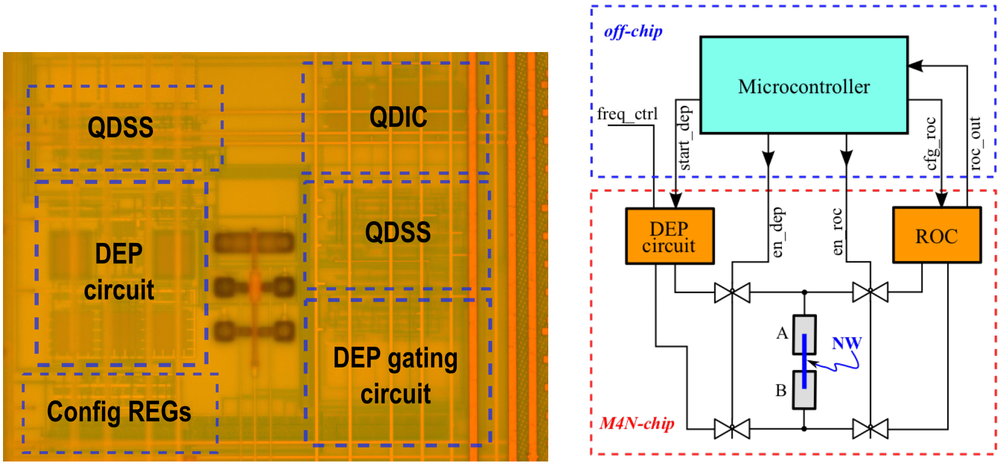

Fig. 3 : Microphotograph and block diagram of the M4N chip. It integrates 3 couples of top gold-electrodes (at the center of image) connected to a Quasi-Digital Impedance Converter (QDIC), two Quasi-Digital Single Slope (QDSS) ADC and a DEP signal generator.

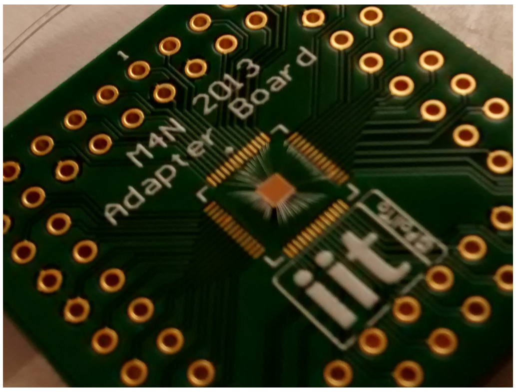

Fig. 4 : M4N prototype bonded using chip-on-board technique. The bondwires are then protected with resin before experiments.

Mixed device-circuit simulations of 6T/8T SRAM cells employing tunnel-FETs

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Introduction. The scaling of the supply voltage V_{DD} is an effective way to reduce power dissipation in digital circuits. The I_{ON}/I_{OFF} ratio in conventional MOSFETs is limited by the thermionic electron emission, corresponding to a minimum sub-threshold swing SS^{min} ~ 60 mV/dec. Novel device architectures based on different operating principles are therefore gaining interest in order to reduce the static power dissipation (lowering I_{OFF} at the same V_{DD}) or the dynamic power (reducing V_{DD} for the same I_{OFF}) without affecting the performance ($\propto I_{ON}$). In the tunnel-FETs (TFETs), the conduction mechanism is the band-to-band tunneling (Fig.1), enabling a sub-60 mV/dec region (Fig.2) as demonstrated by experiments [1]. Among the main issues that may limit the employment of TFETs in digital circuits, we recall the drain current (I_D) unidirectionality and the low I_{ON}.

Simulation methodology. In this work we use idealized TCAD templates for aggressively scaled TFETs and MOSFETs having the same off current I_{OFF}^{LSTP} = 10 pA/um [2][3]. The TFET templates feature a steep sub-60 mV/dec transfer-characteristics over some order of magnitude of current (Fig.2), resulting in I_D larger than in MOSFETs up to V_{GS}~300mV. Various configurations of SRAM cells, namely the 6T and 8T (Fig.3), are used as vehicle circuits to assess how the unidirectionality and small drive current of TFETs impact the operation of this important circuit. Static noise margins (SNMs) as well as write and read delays are computed using mixed device/circuit simulations with the TCAD tool Sentaurus [4][5], in order to compare cell topologies implemented with either MOSFETs or TFETs and for different cell sizing and V_{DD}. Since the 8T is just a 6T cell with two additional transistors for the read, the write operation (and thus the write-SNM and write delay) is the same as the corresponding 6T cell.

Results. Due to unidirectional I_D, there are two possible TFET configurations for the 6T cell according to whether the access-transistor (AT) is inward-facing (IAT, Fig.3a) or outward-facing (OAT, Fig.3b). The IAT configuration does not permit large write and read SNMs (Fig.4a) at the same cell sizing. The OAT configuration, instead, shows nice SNMs (Fig.4b) but, due to unidirectional conduction, has a huge read delay since the OATs are biased with negative V_{DS} during the read (Fig.6, red). Nevertheless, a tradeoff between read SNM and read delay can be found for the 6T OAT cell by pre-charging the bit-lines at $V_{DD}/2$ (Fig.4b and Fig.6, respectively).

Fig.5 shows the write delays for the CMOS cell and the TFET cell (with OAT). Fig.6 compares the read delays of the 6T and 8T cells. TFET-based SRAM cells outperform the related MOSFET cells for V_{DD} below 300÷350 mV, as expected from the I_D characteristics shown in Fig.2. According to the read delay, even if the 8T TFET cell is faster than the 6T one, it extends the window where the TFET cell is advantageous over the MOSFET one by ~ 50 mV but at the cost of two additional transistors. The 6T cell, however, requires pre-charge at $V_{DD}/2$ that is not a conventional biasing of the bit-lines.

Conclusions. Simulations using template devices indicate that TFET-based circuits (the SRAM cell in this study) can outperform the corresponding MOSFET ones only if (at matched off-current) they feature a non-negligible range of V_{GS} where their drain current is larger than in MOSFETs. Appropriate circuit topologies must be used to mitigate the problems associated to the peculiar characteristics of TFETs, such as the unidirectional drain current.

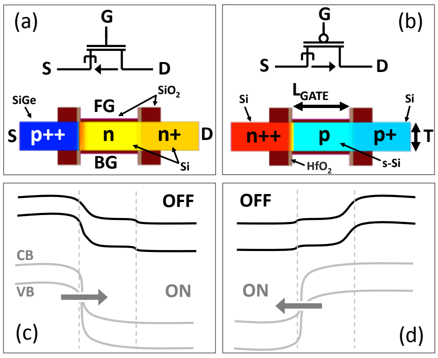

Fig. 1. Structure of the (a) SiGe/Si/Si NTFET and of the (b) Si/strained-Si/Si PTFET. L_{GATE} = 30 nm, T = 10 nm, EOT = 1.1 nm. Details of the device design are provided in [2]. Sketches of band diagrams along the device in both OFF and ON states for the (c) NTFET and the (d) PTFET.

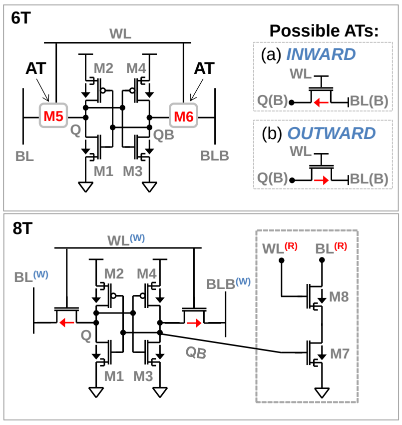

Fig. 3. **(Top)** Symmetric 6T SRAM structures with (a) Inward facing TFET ATs, (b) Outward facing TFET ATs, and **(Bottom)** 8T TFET SRAM cell with Outward-facing write-ATs and two additional nTFETs employed for the read.

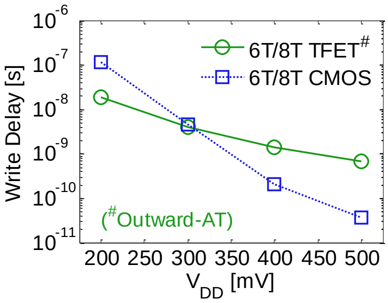

Fig. 5. Comparison of write delays for various supply voltages for TFET SRAM cells (with O-ATs) and CMOS cell.

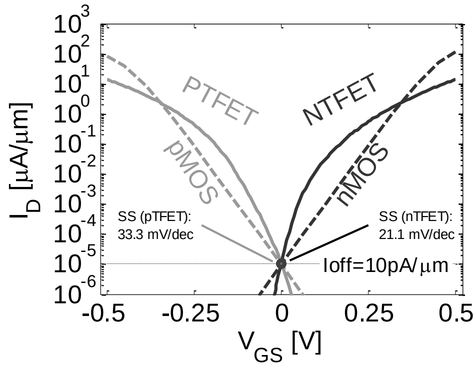

Fig. 2. Simulated I_D-V_{GS} characteristics at $|V_{DS}|$ = 0.5V for the devices in Fig. 1.

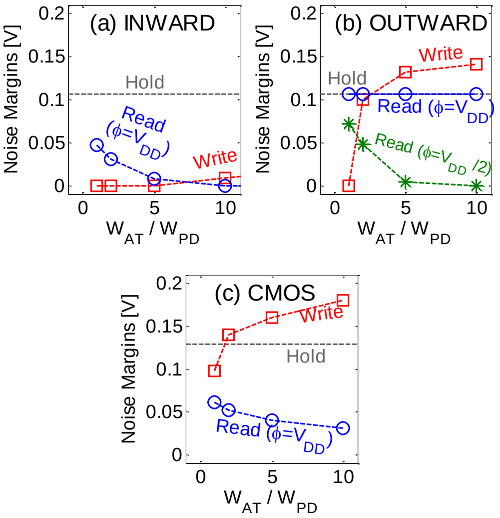

Fig. 4. Hold, Read and Write Static Noise Margins (SNMs) of 6T SRAM cells with (a) Inward-AT TFET, (b) Outward-AT TFET, (c) CMOS cell. V_{DD} = 0.3 V. W_{PU} = W_{PD}.

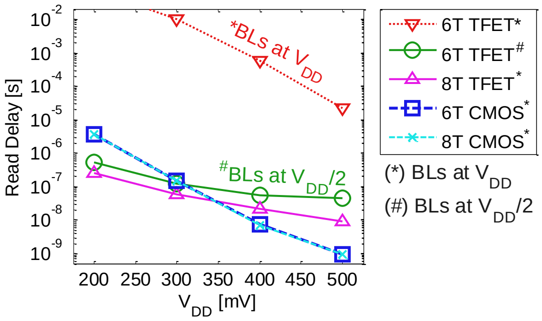

Fig. 6. Comparison of read delays for various supply voltages of the 6T TFET cell (with O-ATs and BLs pre-charge either to V_{DD} or to half V_{DD} for reading), the 8T TFET cell, and the 6T and 8T CMOS cells.

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Modeling of Package Influences on High-Voltage Semiconductor FETs

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Recently, both theoretical and experimental investigations on epoxy resins and polymers have been proposed to understand their propensity to charge transport through carrier injection at the interfaces or due to internal generation processes [1]. The accumulation of charges at the passivation-epoxy interface may lead to electric field distortion within the insulation, passivation and silicon below, leading eventually to leakage currents because of the formation of parasitic transistors [2] or to breakdown instabilities in integrated high-voltage devices [3,4]. Even if charge transport in insulating polymers has been already addressed, physical models suited for commercial TCAD tools are still lacking, thus preventing the application of the available models to realistic IC structures. In addition, no clear explanations on the charge accumulation induced by the wiring within HV-ICs are available. In a recent work, the most relevant features of the charge transport in polymers have been set-up in the Sentaurus SDevice TCAD tool [5]. To this purpose a bipolar transport model has been used based on the Poole-Frenkel effective mobility to emulate the conduction via hopping processes from site to site, which is typical of insulating polymers. Simulations have been compared with experimental data carried out using a dedicated test chip, which incorporates gateless MOS transistors at different distances from the integrated metallization lines carrying the reference high-voltage and ground biases (Fig. 1). The proposed approach is able to predict the features of the leakage current curves measured on different sensors during a complete charging transient (Fig. 2). The sensitivity of high-voltage RESURF LDMOS transistors to parasitic charging in molding compound has been finally investigated by incorporating the passivation and encapsulation layers in the TCAD setup and implementing the conductivity losses in the mold [6]. The role played by field plates and multiple metal/poly-silicon floating rings on the overall RESURF has been revisited by focusing on the breakdown voltage degradation under high-temperature reverse-bias (HTRB) tests. Differently for previous solutions based on MET2 field-plates, a layout re-optimization is proposed for the Triple-RESURF LDMOS device using only MET1and poly-Si levels, which is shown to reach a stable breakdown voltage after long-term HTRB stresses (Fig. 3).

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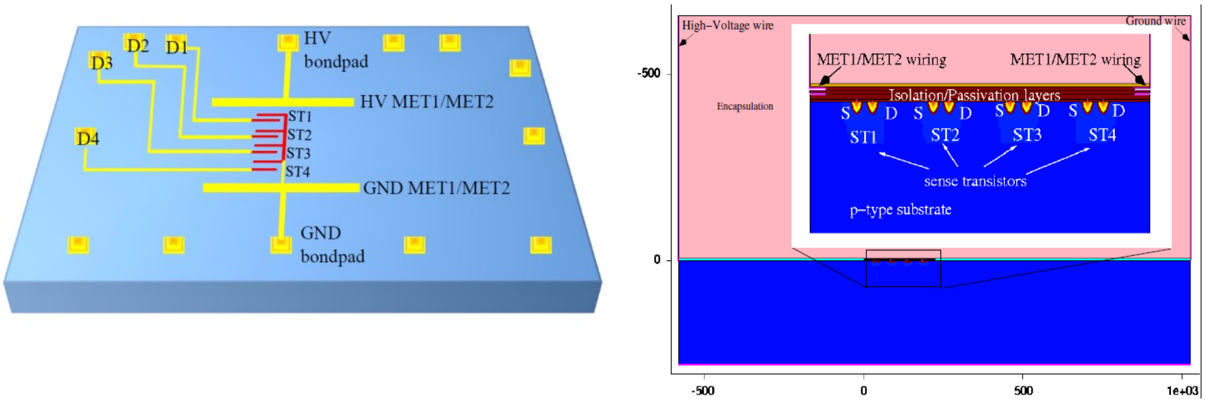

Fig. 1. Left: Structure used for the evaluation of charge creep effects at the molding/passivation interface. Yellow: bondpads and metallizations. Red: n-well mask. Blue: p-type silicon substrate. The distance between HV and GND metallizations is 200 µm, while the distance between sensors is about 40µm. Right: 2D plot of the TCAD deck used for the investigation of the package-induced effects. Inset: zoom of the sensing area. The passivation layers (SiO_2 and SiN) are included in the deck along with the molding resin on top. The HV and ground bondpad wires are realized on the left and right edges of the top region.

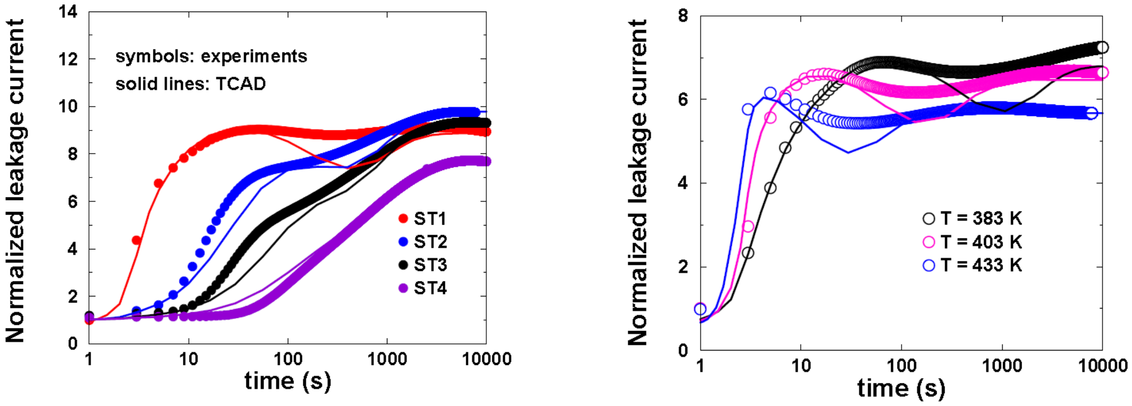

Fig. 2. Left: Normalized leakage current vs. time measured at the drain contact of each sensor during the 210 V dc stress at 393 K. A relatively high-conductivity mold was under investigation. Right: Leakage current at the drain of ST1 vs. time during a 210 V dc stress at different temperatures. Symbols: experiments, lines: TCAD.

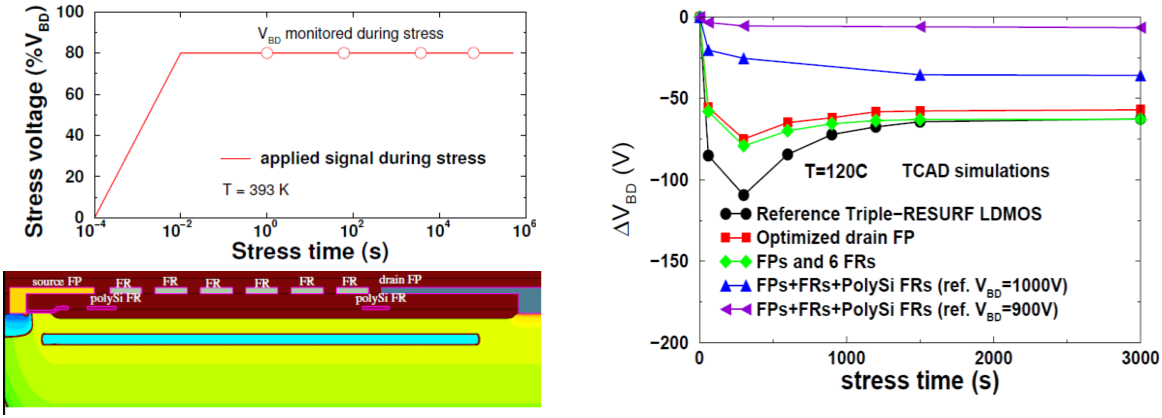

Fig. 3. Left-top: Applied signal during stress. V_{DS} is fixed at 80% of the nominal breakdown voltage V_{BD}. The V_{BD} stability is then monitored at different stress times as in the HTRB test. Simulations were carried out by keeping T = 393 K along the whole procedure. Left-bottom: triple-RESURF LDMOS with field plates (FPs), metal floating rings (FRs) and two additional poly-silicon FRs. The p-type finger limits the beneficial effect of the field plates on top. The poly-silicon FRs redistribute the electrostatic potential along the LDMOS surface preventing breakdown to occur and keeping the potential stable when surface charges accumulate. Right: Optimization of the V_{BD} stability of a 900V triple-RESURF LDMOS. Both longer drain FP and FR configurations have a beneficial effect on V_{BD} (>1000V) but only partially shield the device. The layout solution based on poly-silicon floating-rings under the source and drain field-plate edges is proposed for two devices with V_{BD} = 1000 V and 900V, respectively, showing significantly improved HTRB stability.

Novel high-voltage double-pulsed system for GaN-based power HEMTs

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Abstract. This paper presents a fully customable high-voltage pulsed system capable of double-pulsed I-V and time-resolved drain-current transient characterization from 1µs to 100s range. The system allows a comprehensive characterization of charge-trapping phenomena affecting the dynamic performances of GaN power HEMTs under high-voltage regimes.

Introduction. GaN-based High Electron Mobility Transistors represent excellent devices for the realization of next-generation power switching systems [1-3]. Nevertheless, the dynamic behaviour of these devices can be limited by the presence of deep trap-states, which may promote the collapse of dynamic performances and contribute to the onset of premature breakdown mechanisms [4]. For this reason, as the operational bias condition is approaching relatively high-voltage ranges, the upgrading of time-resolved characterization systems is of primary importance in order to investigate the unexplored high-voltage trapping mechanisms. In this work, we present a high-voltage high-speed pulsed measurement system capable of double-pulsed I-V and current transient characterizations, complementary and crucial techniques for the investigation of current dispersion phenomena and for the identification of related trap-states [5-6].

Description. The proposed system includes: (i) two low-power pulse generators; (ii) one (optionally two) high-speed power amplifier(s) needed for the high-voltage pulses amplification; (iii) a current-sensing resistor, (iv) a high-voltage differential probe, and (v) a low-power signal acquisition module for the current/voltage capturing (see Figure 1).

The main advantages of the proposed setup are here summarized. At first, conversely to the conventional gate-lag technique, the transient characterization methodology inherits the advantages of the double-pulse system (i) attenuating the load-line constrains between trapping and measuring phases and (ii) mitigating the detrimental bias variations caused by the dynamic de-trapping processes. Second, the consistency of time-resolved data acquisition is guaranteed throughout a wide time-span from 1µs to 100s, thanks to the extremely large memory-depth of modern acquisition modules. Third, thanks to the high-voltage differential probing, the front-end stage of the acquisition module in not directly connected to the high-voltage drain terminal, making the acquisition of the voltage signals easier. This setup can work at maximum drain voltage of 200V, sufficient for standard RF devices, or it can be upgraded up to 600V system to fit the actual requirements of GaN power transistors.

Results. To demonstrate the effectiveness of the proposed system, double-pulsed I_D-V_D characterization and dynamic R_{ON} recovery transients have been performed on a preliminary technology of AlGaN/GaN Schottky-gate power HEMTs. From pulsed I_D-V_D curves (see Figure 4) it can be observed that the device experiences a dramatic increase of the dynamic R_{ON} collapse as the quiescent drain-voltage increases from 50V to 200V. Time-resolved R_{ON} transients reveal the presence of three distinct charge de-trapping processes which amplitudes are well correlated with the quiescent off-state drain-voltage (see Figure 5). This result suggests that the R_{ON}-collapse is promoted by charge-trapping into three deep-levels triggered by different voltage biases.

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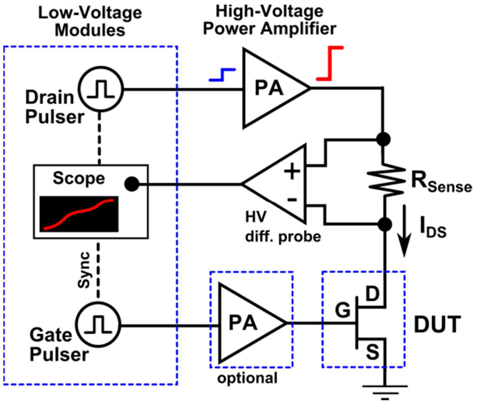

Figure 1: Schematic diagram of the proposed high-voltage double-pulsed system, including the low-voltage pulse generators, the high-speed power amplifiers, the high-voltage differential probe and the oscilloscope.

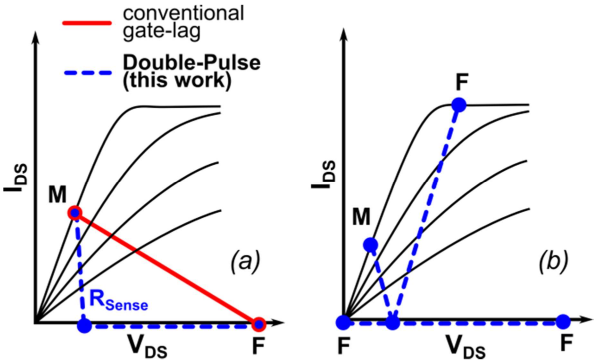

Figure 2: Comparison between the conventional fixed-V_{DD} gate-lag technique (a), and the proposed double-pulsed technique (b). The latter allows the releasing of the load-line constrains and the de-coupling of Filling/Measuring (F/M) bias-pairs. In (b), examples of F/M bias-points requiring negative load-resistors.

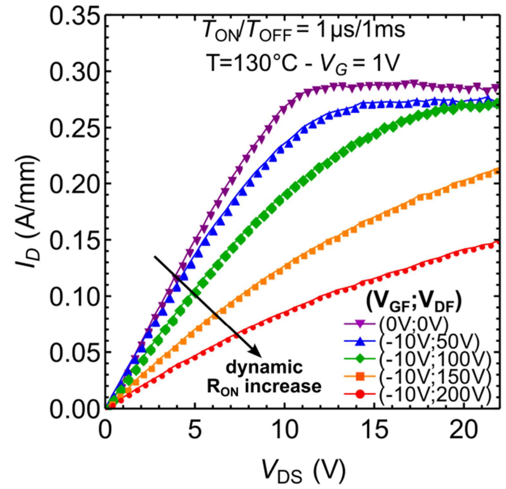

Figure 4: Double-pulsed I_D-V_D characterization with high-voltage off-state (V_{GF};V_{DF}) quiescent bias-points. As the quiescent drain-voltage exceeds 50V, the device experiences a dramatic increase of the dynamic R_{ON}.

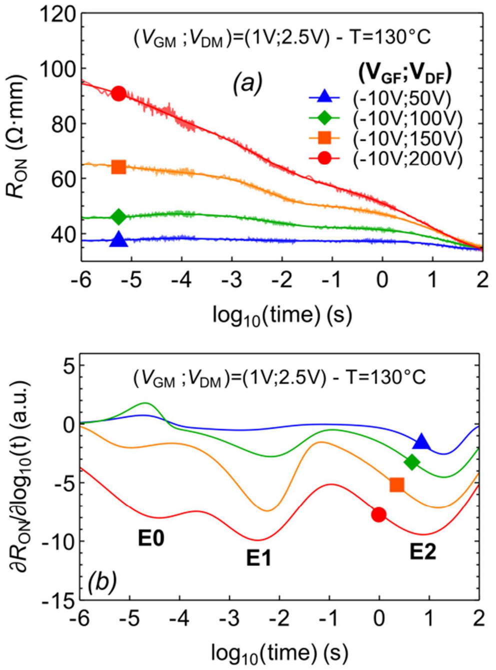

Figure 5: (a) Time-resolved dynamic R_{ON} recovery transients, and (b) derivative of the stretched-exponential fit-functions, employed to extrapolate the three distinct deep-levels signatures corresponding to three charge (de)trapping processes. As the filling drain-voltage increases from 50V to 200V, the increase of E0 and E1 peak-amplitudes can be observed.

On the investigation of ESD Failure mechanisms in AlGaN/GaN RF HEMTs

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Introduction: GaN based High Electron Mobility Transistors (HEMTs) demonstrate superior performance in high power and frequency applications [1]. Although the high breakdown field (3.3 MV/cm), GaN transistors significantly suffer from electrostatic discharge effects (ESD) [2],[3]. The aim of this paper is to present an investigation of the ESD effects on GaN HEMTs in order to discriminate field- and power- dependent mechanisms when different gate voltage levels are used. Robustness toward vertical breakdown is further investigated.

Analysis of field- and power- dependent mechanisms: ESD investigation was performed on AlGaN/GaN HEMTs with W_G=2x50 µm, L_G=2 µm, L_{GD}=8 µm. Tests were performed with a time domain reflection transmission line pulse (TDR-TLP) custom setup [4], biasing the devices with 100ns rectangular pulses at different gate voltage levels from V_G=-10V to V_G=1V. After each pulse dc main parameters were monitored. Figure 1 reports, for a representative device tested in on-state (left) and off-state (right), I-V TLP curves (black line); the corresponding leakage drain current (I_{dleak}) monitored after each TLP pulse at V_D=4V, V_G=-6V is shown (red line). Figure 2 clarifies that the failure voltage has two main trends: (i) during on-state TLP testing, a power dependent mechanism dominates and the failure voltage follows a iso-power curve; (ii) during off-state TLP testing, failure depends on a field-dependent process, revealing negligible change in voltage failure (≈ 300V) when different V_G values are applied. The correlation between the drain failure voltage and the current measured during TLP pulse just before failure confirms the presence of the two mechanisms.

Soft breakdown at high power dissipation conditions: TLP testing at high power dissipation conditions (V_G=0V, V_G=1V) reports soft breakdown before catastrophic failure, mainly described by a significant gate current increase. The degradation of the gate is further confirmed by dc analysis (Figure 3), revealing a significant increase of the diode forward and reverse current and a degradation of the I_DV_D curves. Emission microscopy (Figure 4) shows that after soft breakdown “hot spots” are created, suggesting the creation or enhancement of leakage paths under the gate during gate degradation.

Vertical breakdown: The origin of failure detected during off-state TLP testing (i.e. lateral or vertical breakdown mechanism) was studied with drain to substrate TLP tests, keeping both source and gate terminals floating. The significant increase of the robustness measured in this configuration (no catastrophic failure up to 450V (Figure 5)) suggests that vertical breakdown has no influence on catastrophic failure observed during off-state TLP testing.

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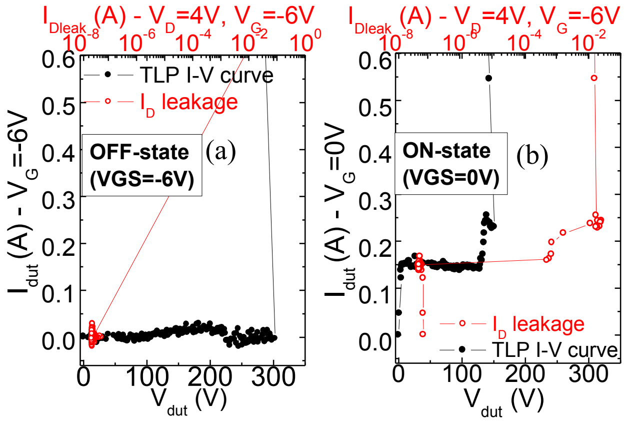

Figure 1: I-V TLP curve (black) and corresponding I_{Dleak} monitored after each TLP pulse (red) at drain voltage V_D=4V, gate voltage V_G=-6V.

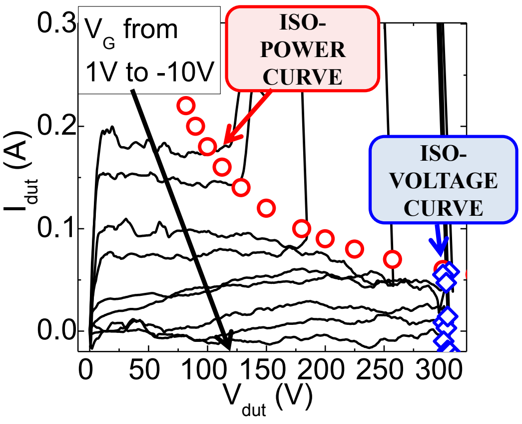

Figure 2: I-V TLP curve monitored during TLP testing at different gate voltage levels (from +1V to -10V)

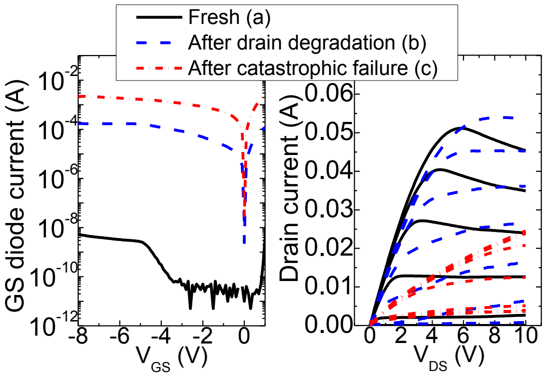

Figure 3: Comparison of dc curves measured on a AlGaN/GaN HEMT before (a), after degradation (b) and catastrophic failure (c).

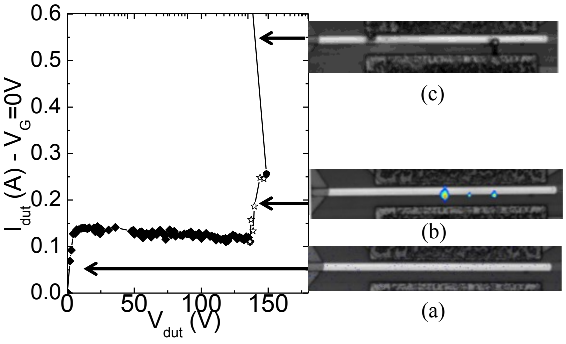

Figure 4: Light emission corresponding to TLP testing at V_G=0V.

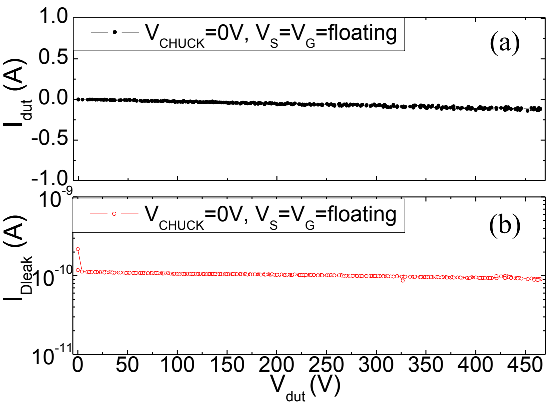

Figure 5: I-V TLP curve during drain to substrate TLP testing (a). Corresponding leakage drain current (b).

Pressure-Triggered Non-Volatile Memory Devices Based on Organic/Inorganic Nanocomposites

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The continuous development of the information industry is leading to a growing demand for new-generation data-storage technologies. Recently, increasing attention has been paid to applications in memory devices based on organic materials: thanks to the advantages of good scalability, flexibility, low cost and ease of processing, organic memories seem to be a promising alternative or supplementary devices to conventional inorganic memory technology [1]. In particular, resistive memory devices have been attracting significant interests due mainly to their simple structure. The basic feature of an organic resistive memory is to exhibit a bistable behaviour: such kind of device possesses two stable resistance states which can be reversibly modulated by external electrical stimulation. So far, many groups have demonstrated the resistive switching in several types of organic and polymeric materials with different device structures [2, 3, 4].

In this work we present a non-volatile resistive memory device based on a new combination of materials. Each memory element is obtained by sandwiching a hybrid organic/inorganic active layer between two metal electrodes. The active layer is a nanocomposite material made of an organic semiconductor and metal nanoparticles (NPs). In particular, a perylene-derivative with extraordinary stability in air, namely (Figure 1) ActiveInk^{TM} N1400 (Polyera), is employed as organic semiconductor, while gold or aluminum are employed for the NPs interlayer. In a first step, the memories were fabricated on glass substrates, later all the technology has been transferred successfully on plastic substrates.

The memory devices showed a reproducible behavior (Figure 2), with on/off current ratio usually ranging around 10^3-10^4 and remarkably long retention times of more than $2.6 \cdot 10^7$ seconds (10 months). The devices have been tested and stored in air for the whole duration of the investigation, and they showed more than 2 years of global lifetime. In order to shed light onto the switching mechanism, a morphological characterization of the hybrid nanocomposite was also performed. It will be shown that such a resistive switching seems to be induced by the formation of metallic filaments inside the hybrid matrix, and that this behaviour is triggered by the presence of metallic nanoparticles dispersed into the organic layer.

Finally, the integration of the memory elements with electrical sensors was successfully realized. Since resistive memories respond to an applied voltage by a non-volatile change of the conductivity, an external stimulus from a sensor element can be used to induce the memory device to switch. In particular, if a memory element is connected in series with a piezoresistor, the resistivity change in the piezoresistor, induced by an external pressure, can be used for triggering the memory, creating a novel sensor-memory system (Figure 3).

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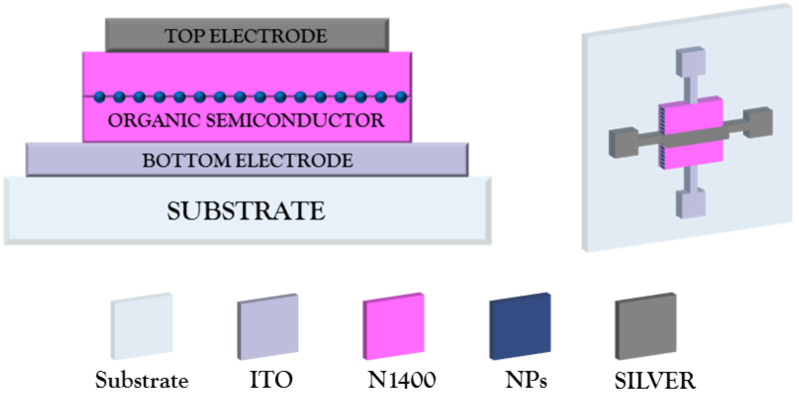

Figure 1: Schematic view of the layered memory element.

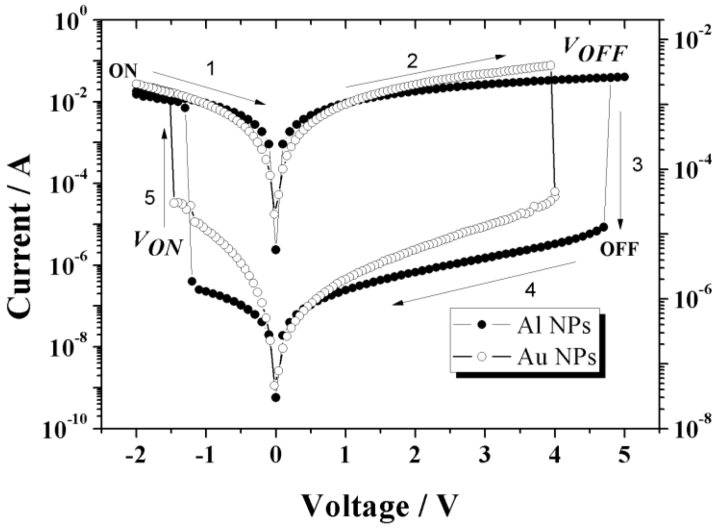

Figure 2: Typical I–V curves (the lefty-axis is referred to the Al-NPs based memories and the right one is referred to the Au NPs based memories).

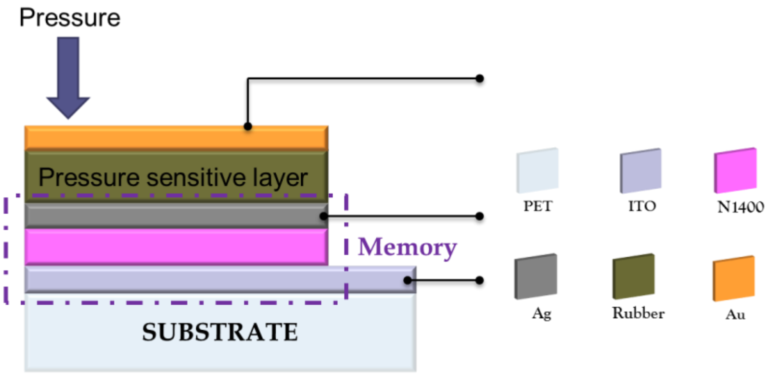

Figura 3: Schematic representation of the integration of 1 memory element and 1 pressure sensor

Study and fabrication of selected organic electronic devices to improve performance and stability

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Over the last years, organic electronics has performed enormous progresses; in particular, organic light emitting diodes (OLEDs) have been intensively studied due to their potential application in flat-panel displays and flexible systems. The best performances have been achieved employing phosphorescent materials as emitters. However, some problems remain related to the stability and chromaticity of devices incorporating blue phosphorescent dyes [1]. In our research, we have realized blue OLEDs exploiting α-NPD, a well-known fluorescent molecule, both as hole transport layer (HTL) and emitting layer (EML) [2], thus simplifying devices structure and avoiding the adoption of blue phosphorescent materials. This approach can be extended to white hybrid OLED architectures (Fig. 1a).

Besides stability problems related to blue phosphorescent emitters, short OLED lifetime is still a major challenge to the commercial diffusion of these devices. Two different mechanisms can worsen the OLED performance: intrinsic or extrinsic degradation [3]. Recently, we have studied intrinsic degradation phenomena focusing on shelf life analysis, performing experiments at different storage conditions on two types of blue OLEDs (Fig. 1) [4].

The critical issue of stability improvement is also perceived for other several devices, like organic thin film transistors (OTFTs), where stable n-type semiconductors are rare but of great significance for the development of CMOS-like devices. We have studied fullerene C_{60}, applying different process conditions and treatments of the interfaces [5]. The morphological properties of the fullerene layers have been observed and the electrical characteristics of the transistors (Fig. 2) have been analyzed.

Since OTFTs can be integrated in optoelectronic applications, as part of driving circuitry of displays, or used as photo-detectors or light activated memory devices, it is also important to understand the effect of illumination on their electrical performances [6]. For this reason, our study has focused on the development of equations modeling the effect of long-lived traps [7] and the relation between the threshold voltage shift, the bias and the illumination time (Fig. 3).

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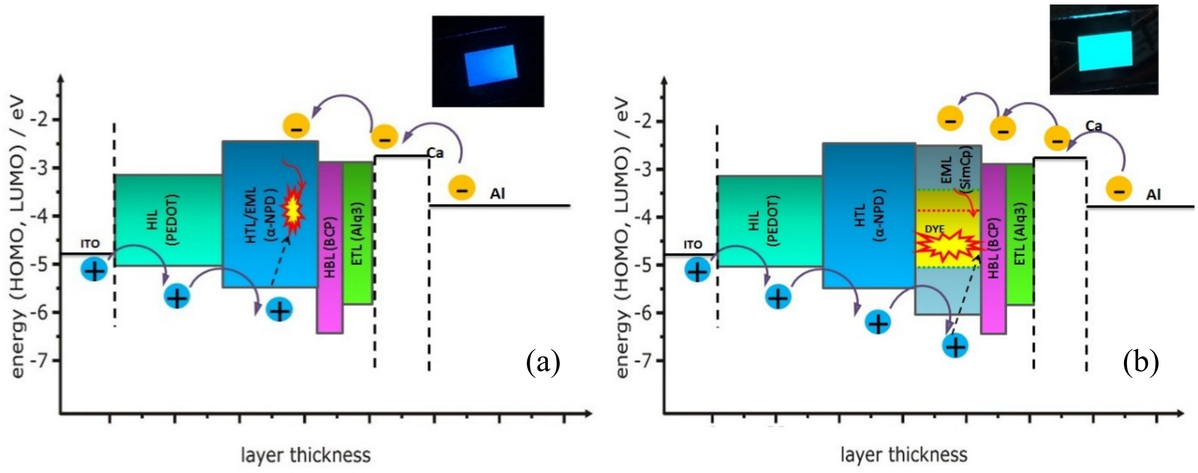

Figure 1: Energy levels of multilayer OLEDs. (a) Fluorescent blue OLED structure and (inset) working encapsulated device. From anode (ITO): hole injection layer (HIL), hole transport layer / fluorescent emitting layer (HTL/EML), hole blocking layer (HBL), electron transport layer (ETL), cathode (Ca/Al). (b) Phosphorescent blue OLED structure and (inset) encapsulated working device. HTL and EML are here split in two different layers. Only OLEDs based on phosphorescent emitting molecules can achieve a theoretical internal quantum efficiency of 100%, because both singlet and triplet excitons contribute to light emission. Devices of both types have been stored at different conditions and measured periodically pointing out OLED degradation at shelf life conditions for both fluorescent and phosphorescent devices.

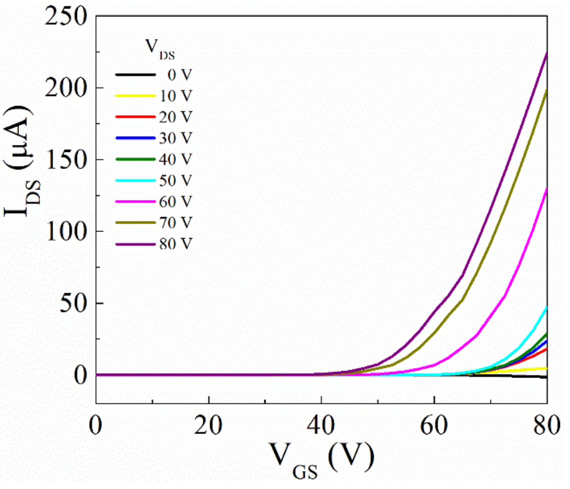

Figure 2: Typical transfer characteristics of a fabricated C_{60} OTFT. Device architecture is bottom-gate bottom-contacts: the substrate is a Si/SiO$_2$ wafer (oxide thickness 200 nm), source and drain are made of gold (50 nm), with interdigitated configuration and W/L = 550. Semiconductor thickness is 80 nm. Before C_{60} deposition, an UV/ozone cleaning is performed with different exposure times and then HMDS SAM is deposited.

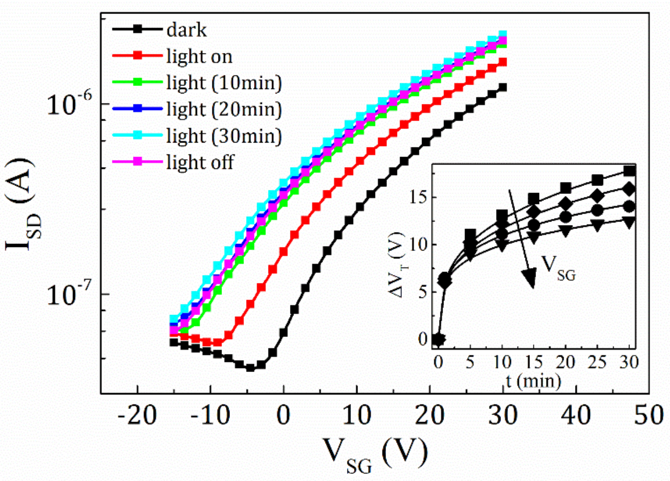

Figure 3: Transfer curves of a pentacene-based OTFT in dark, under light and after irradiation. During illumination, a gradual shift of the threshold voltage was observed, suggesting that an even larger number of photogenerated carriers are being trapped in the semiconductor at the interface with insulator and contacts. The translation in V_T showed to be slower for high negative V_{GS}, due to the repulsion of electrons and the enhanced recombination of holes.

Transport modeling challenges for GaN-based light-emitting diodes

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The challenges posed by the numerical modeling of GaN-based light-emitting diodes (LEDs) require the extension of current simulation approaches beyond the semiclassical limits. Any theory hoping to predict the complex carrier transport and optical properties of state-of-the-art III-nitride LEDs should combine a genuine quantum approach with an atomistic description of the electronic structure. However, practical computational considerations have motivated the inclusion of quantum corrections within the semiclassical drift-diffusion (DD) framework. As an example of satisfactory application of such a hybrid approach, we have investigated numerically the role played by defects in the device active region not only as non-radiative recombination centers but also in terms of trap-assisted tunneling (TAT). TAT can be globally viewed as a sequence of three processes (see Fig. 1). We have accurately reproduced the electrical characteristics of different LED structures [1,2] by including electron and hole tunneling features such as nonlocality and multiphonon emission through appropriate expressions of capture rates within a SRH-like recombination rate [3].

Overly optimistic conclusions from these encouraging results have to be tempered when comparing commercial simulators implementing quantum-corrected DD for the calculation of carrier transport across the active region of GaN LEDs (in the present work, we have considered Crosslight APSYS and Synopsys TCAD Sentaurus). All semiclassical descriptions of carrier transport across QWs involve the separation between unconfined and confined populations, described by three- and two-dimensional (3D, 2D) carrier densities, respectively. The two populations are coupled by electrostatics (the selfconsistent solution of the Poisson and Schrödinger equations, PSEs) and by carrier capture/escape processes. Commercial codes use different algorithms for determining the extension of the region where PSEs are solved, adopt different boundary conditions for the Schrödinger equation, and use the PSE results in the DD model in subtly different ways inside and outside the QWs. The cumulative effects of these differences can be observed in Fig. 3, where the perfect agreement between the *I(V)* curves obtained from classical DD simulations with APSYS and Sentaurus gives place to significant differences at all bias regimes when PSEs and DD are coupled.

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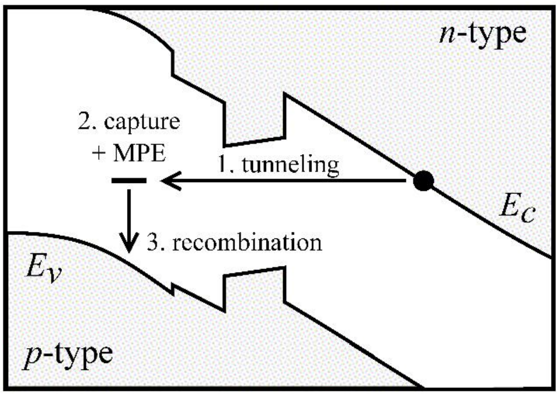

Figure 1: Schematic description of a TAT process for electrons across the active region of a SQW LED. The tunneling current is determined by the contribution of three different processes (and their respective probabilities): 1. pure tunneling; 2. capture by the trap and multiphonon emission (MPE); 3. non-radiative recombination with holes in the valence band in the p-type side. The opposite process can occur for holes towards defects in the *n*-type side of the diode.

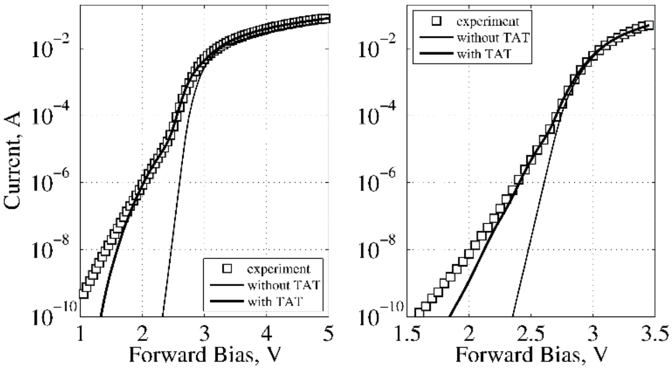

Figure 2: Room temperature comparisons between measured and simulated characteristics with and without TAT for two SQW test LED structures manufactured by OSRAM Opto Semiconductors (left: SiC substrate [1], right: Si substrate [1]).

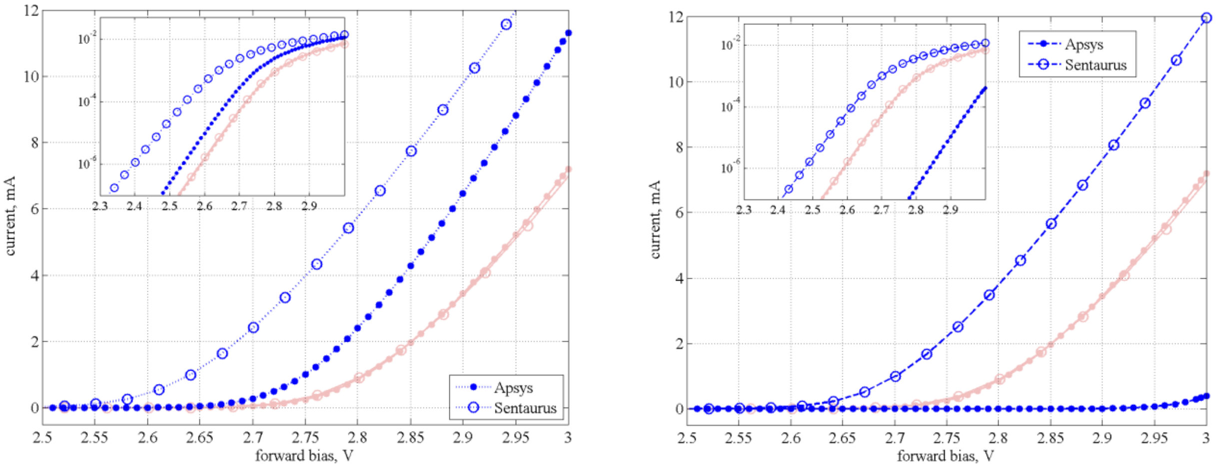

Figure 3. *I(V)* characteristics of a SQW test LED structure [2] simulated with Crosslight APSYS and Synopsys TCAD Sentaurus. (The same curves are reported in logarithmic scale in the insets.) While a perfect match is obtained with classical DD simulations (red curves), the inclusion of quantum corrections leads to significant differences at all bias regimes. The results of both simulators are also extremely sensitive to the extension of the region where the PSE are solved, as can be noticed by comparing the curves on the left (wider PSE domain, extending 1.5 nm beyond the SWQ heterointerfaces) and on the right (narrower PSE domain, extending just 0.2 nm outside the SQW edges).

An Ultra-Wideband Monolithic Active Balun

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Many Ultra-WideBand Electronic Warfare (UWB EW) systems cover the band from 0.5 GHz to 18.0 GHz, which corresponds to a relative bandwidth of 36:1. Such multi-octave systems often require critical design of RF components and circuits. One of the key issues for UWB EW systems is the realization of directional antennas for a multioctave bandwidth. To this purpose, a planar self-complementary antenna design approach has demonstrated significant performances. This solution provides differential mode signal with an output impedance of 60π ohms, which is one half of the space impedance. The output signal of the antenna requires RF broadband front-end modules with an input overload protection, an amplification stage, a Balun and an high impedance drive with minimized group delays.

For UWB applications, several broadband amplifiers with a non-zero common mode amplification have been reported in the literature [1], while it is difficult to design wideband Baluns, impedance transformers and overload protection circuits with passive components and of miniaturized size [2-3]. To solve these issues, we have integrated the four functions necessary to match the receiver to the UWB radiating element into a single MMIC that covers the 0.5-18GHz frequency bandwidth [4]. The UWB microwave limiter, low noise amplifier, balanced to single-ended adapter and impedance transformer are all included in the MMIC. This allows the realization of a product with a high integration factor that reduces costs and sizes. The MMIC has a gain of 13 dB in the full band, with a reduced noise figure of 4.5dB, better than 20 dB common-mode rejection and 30 dBm input overload protection. In addition, the circuit has a single bias from the output port, that greatly simplifies its use within the receiving system. The total power consumption is 20mW, with a total current of 35mA at 6V, while the chip dimensions are 2x4mm.

The MMIC has been simulated and manufactured using the model library of a commercial GaAs pHEMT foundry. The technology chosen for the design is the 0.15μm Power PHEMT 3MI from TriQuint, with transition frequency at 80 GHz. Simulation and measurements of the MMIC are in good agreement, demonstrating the feasibility of the approach. The general scheme of the active Balun is shown in Fig. 1, while in Fig. 2a a photo of the chip is presented. It has been glued in a test jig with SMA connectors and two access microstrip lines (Fig.2b). In Fig. 3 the simulated and measured S-parameters are shown.

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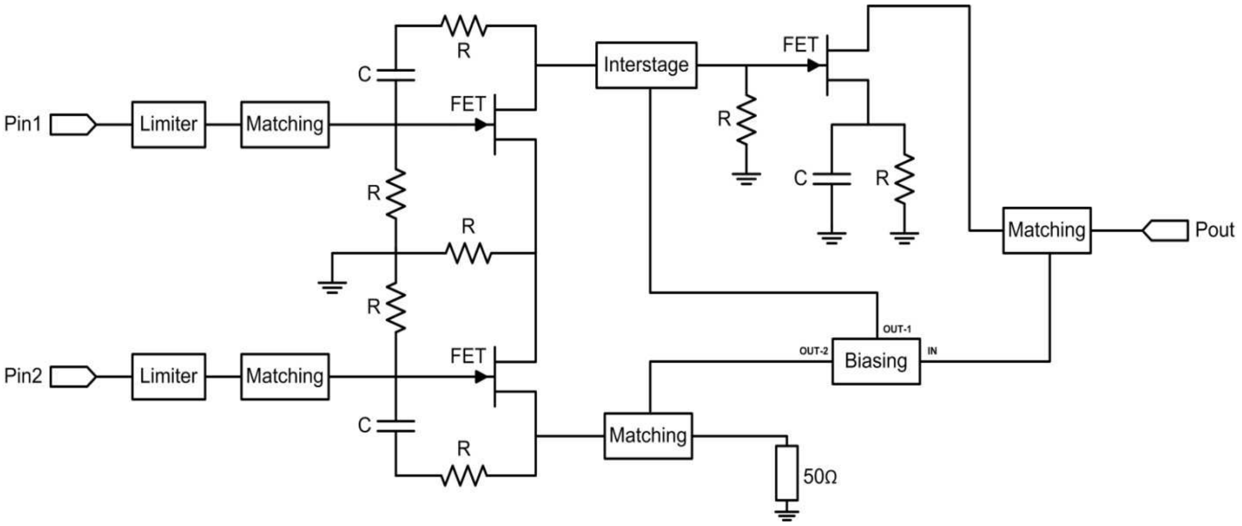
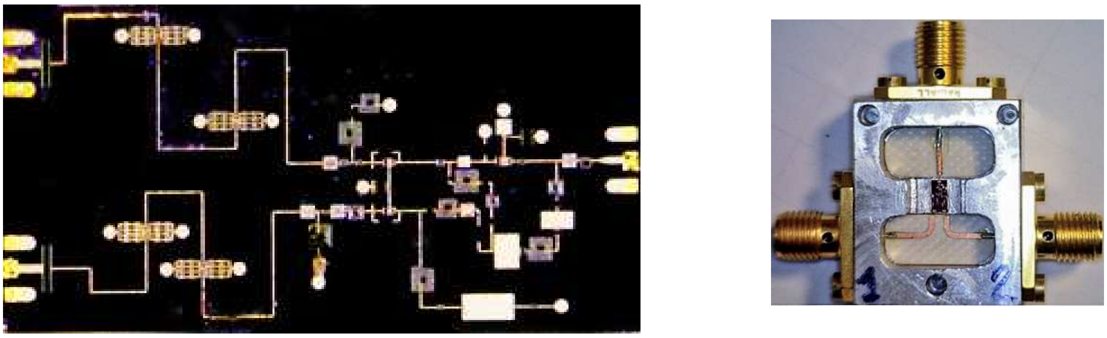


Fig. 1 A simplified schematic of the active Balun.



(a) (b)

Fig. 2 (a) A photo of the active Balun chip; (b) The chip inside the test jig.

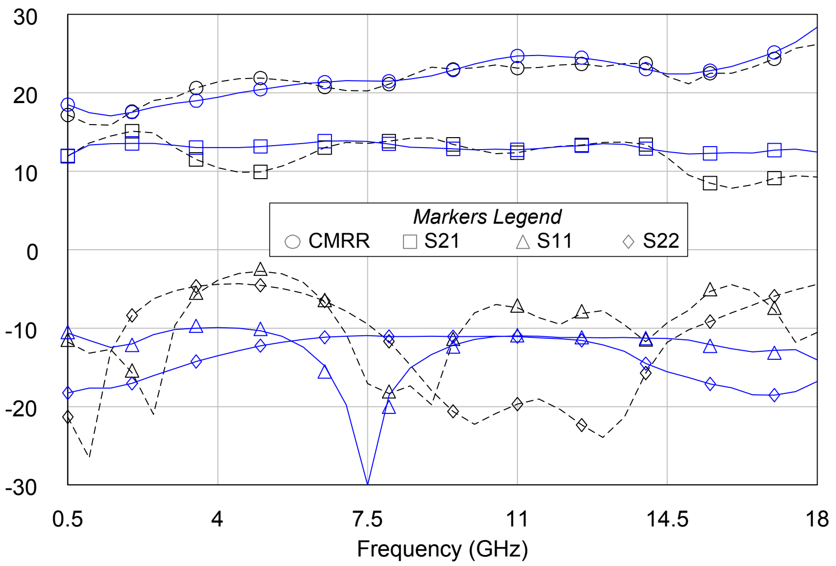


Fig. 3 Simulated (solid lines) and measured (dashed lines) S-parameters of the Balun, for the difference and common mode.

Development of a 230W SSPA for Galileo Satellite System

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A satellite is a complex system with a huge number of electronic components working in harsh environmental conditions. Thus, robustness and reliability are key characteristics that have to be guarantee to assure the overall success of the mission. Moreover, due to the high cost per kilogram of the payload, space and weight of every subsystems have to be reduced as much as possible to maximize the cost-benefits trade-off of the mission. Therefore, the design of space borne microwave components is usually the result of a compromise among several aspects. In this context, the power amplifier represents the most critical block since it heavy affects mass, dc power consumption, thermal and mechanical management. Actually, Traveling Wave Tube Amplifiers (TWTAs) are still the preferred solution in almost every bands due to their relevant RF power capability. On the other hand, TWTAs required very high dc voltages and expensive realization processes to avoid multipaction and corona effects. Moreover, they need large volume and heaviness especially in the lower frequency bands such as L and S.

Nowadays, with the development of wide band gap solid-state technologies such as GaN HEMT, Solid State Power Amplifiers (SSPAs) start becoming valid alternatives to replace TWTAs also in satellites requiring very high level of RF power. In fact, GaN technology provides transistors with ten times higher power density as compared to Gallium Arsenide devices. This makes possible the realization of power amplifiers with electric characteristics similar or even better than the ones of the TWTAs but with smaller size and mass.

With this aim, the main steps carried out for the development of an L-Band high power and efficient SSPA designed for the European satellite navigation system (i.e., Galileo) are described. The SSPA has been developed in the framework of an European Project named SLOGAN, and it exploits the GH50-10 GaN technology provided by United Monolithic Semiconductor foundry. The consortium of the SLOGAN project is composed of six partners European partners from industry and academy, among which our team is responsible of the design, realization and characterization of the whole radio frequency unit (RFU) [1]. The idea is to offer a valid alternative to replace TWTA with more compact and reliable systems. All the SSPA functionalities, i.e. power supply, power conditioning and RF amplification, are integrated in the developed architecture and accommodate in a unique box with limited volume and mass. In particular, the required output power level is achieved by parallelizing several GaN die power bars of 26.5 mm.

The developed RFU architecture is divided in three main units: a High Power Amplifier (HPA), a Driver stage and a Gain Control Unit (GCU). The HPA unit is realized through the parallel combination of 4 modules able to deliver 80 W of output power each. These four amplifiers are joined at the input and at the output through an ad-hoc designed input power splitter (IPS) and output power combiner (OPC), respectively. The HPA is driven by two driver stages able to provide 40 dB of linear gain in the overall bandwidth. The RFU is completed by the GCU that is devoted to control the overall gain and to allow its compensation over temperature and aging effects. A picture of the first prototype, without the GCU, is shown in figure 1.

Figure 2 shows the registered performance at the center frequency (i.e., 1.575.42 GHz), in continuous wave operating mode. As can be noted, the prototype is able to deliver an output power higher than 54 dBm at less than 2 dB of gain compression. Moreover, the registered gain and efficiency are higher than 54 dB and 54%, respectively.

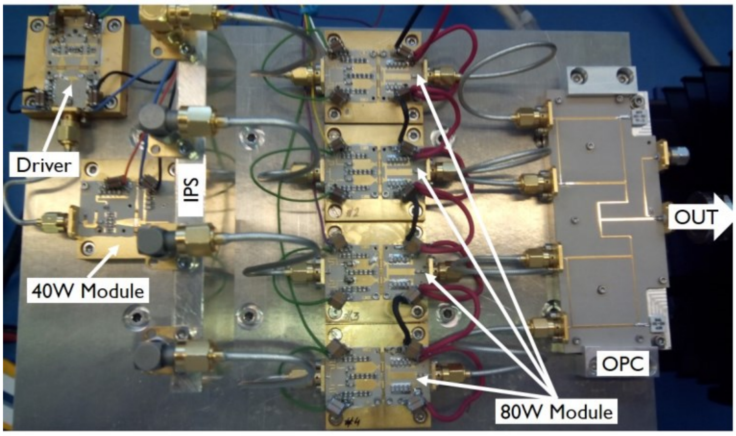

Figure 1: Picture of the first developed prototype.

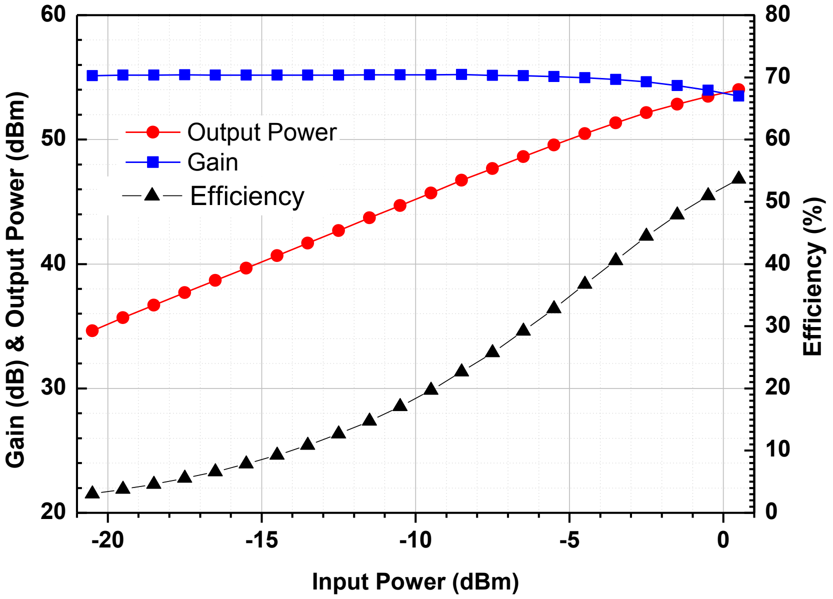

Figure 2: Performance of the first prototype at the center frequency, f_0=1575.42GHz.

ACKNOWLEDGMENT

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Distributed architecture for logarithmic amplifications

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Radar systems are affected from saturation of the receiver chain. A possible solution consists on using automatic gain control systems but they reduce sensitivity, therefore weak signals get lost. A simple and performing solution to overcome such drawback is represented by logarithmic amplifiers (LAs). Three kind of LAs can be reported: True Logarithmic Amplifier (TLA), Detection Logarithmic Video Amplifier (DLVAs) and Successive Detection Logarithmic Video Amplifier (SDLVAs)[1]-[2]. DLVAs and SDLVAs extract the signal envelop directly, in particular SDLVAs are characterized by a typical high Input Dynamic Range (IDR). Another important parameter for radar systems is robustness [3]-[4], which is improved by GaN technology. This contribution proposes a novel high IDR GaN wideband architecture.

The typical SDLVA architecture is shown in Figure 1 and is composed by a linear amplifying chain cascaded by detectors, limiters and a summing node. Each detector works with the same input power but for a different portion of the whole IDR. In such a way, the video output signal reconstructs the logarithmic response, as visible in Figure 2. Several trade-offs have to be taken into account. The single linear amplifier gain is responsible essentially for the IDR and the Logarithmic Error (LE). The detector limiting voltage value affects the Logarithmic Slope (LS), thus the output voltage range. In addition, power consumption considerations have to be accounted. To size the LA, any of such aspects can be summarized as in Table 1. Once the detector dynamic range is obtained, as visible in Figure 3, it is possible to choose one of the row of Table 1. In particular, the third row has been chosen in this work, thus predicting a ±1.35 dB LE, a 60 dB IDR and the need of 6 detectors (5 linear amplifiers). A worsening of such values has to be foreseen, because the TSS affects the IDR while the chosen architecture affects the LE.

The single LA section is shown in Figure 4. A four-FETs DA [5] is terminated on the detector on the gate line, while the drain line includes the next section or the last detector according to an intermediate section or the final one. Each DA has to provide 10 dB gain, and simulated results are visible in Figure 5, in which the 10 dB distance step among each amplifier is achieved. Putting together the linear chain and detectors, performance in Figure 6 is expected, which means a ±1.7 dB LE at 10 GHz. By sweeping frequency over the 3-17 GHz range, a further deviation of ±0.9 dB occurs. The IDR is 55 dB, in the range -45÷10 dBm. Chip size is 5.2x6.2 mm^2 and 6.2 W power consumption is required. Chip layout is shown in Figure 7.

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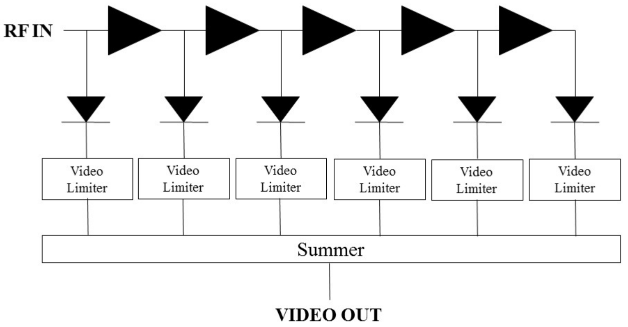

Figure 1: SDLVA architecture.

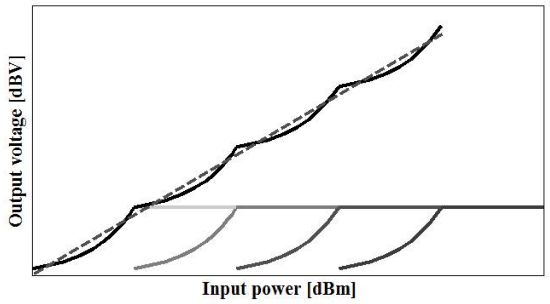

Figure 2: Logarithmic response reconstruction.

Table 1: SDLVA sizing table.

Detector DR [dB]	Log. Error [dB]	Number of detectors	SDLVA IDR [dB]
8	±0.89	8	64
9	±1.10	7	63
10	±1.35	6	60
11	±1.60	5	55
12	±1.88	5	60
13	±2.18	5	65
14	±2.49	4	56
15	±2.81	4	60

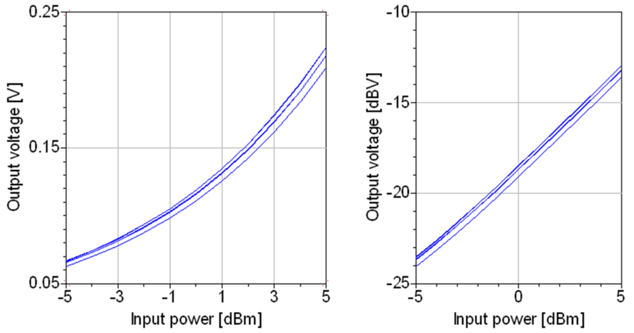

Figure 3: Detector performance in linear (left) and logarithmic (right) output voltage *vs* input power.

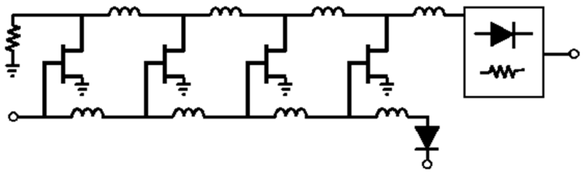

Figure 4: Single LA section.

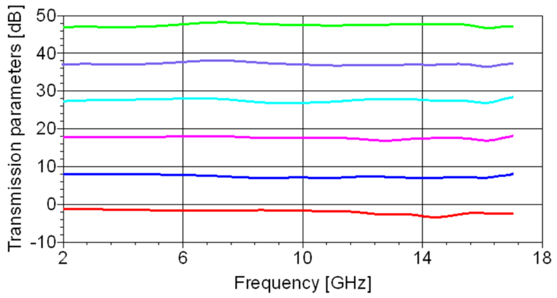

Figure 5: Transmission parameter of each DA on the linear chain.

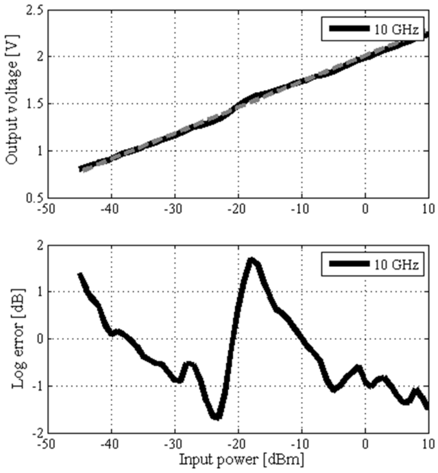

Figure 6: Expected logarithmic amplifier performance. Output voltage vs input power (top) and corresponding logarithmic error (bottom) at 10 GHz.

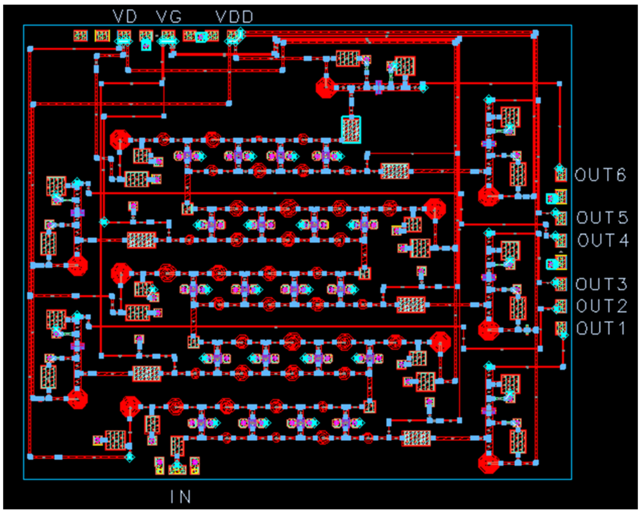

Figure 7: LA layout.

Fabrication and characterization of graphene field effect transistors (GFET)

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Graphene is a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice. This peculiarity is responsible of extraordinary physical properties. Graphene exhibits a strong ambipolar field effect and thanks to its huge charge carrier mobility, graphene is a suitable material for high frequency Electronics [1-2]. Graphene field effect transistors (GFET) for high frequency applications have recently received much attention and significant progress has been achieved in this area. GFETs have been already made by using pre-patterned metal or graphene nanoribbon (GNR) back-gates and hexagonal boron nitride as a dielectric spacer [3]. Among the most employed techniques for the graphene transfer, i.e. mechanical exfoliation, chemical exfoliation and chemical vapor deposition (CVD) growth, the latter has the advantage to produce several devices on the same chip with a very high yield. In this work, we focus on the characterization of a novel generation of GFETs, in which a graphene sheet, grown via CVD, is used as channel material.

Our devices were built on a sapphire substrate using aluminium oxide (Al_2O_3) as dielectric layer. Several specimens were fabricated with different gate lengths, ranging from 1μm to 2μm, but with the same channel length (2.4μm). The devices pattern is shown in Fig.1. The first fabrication step consists in building the back gate with the two gate fingers for modulating the Fermi level in the graphene sheet. The back gate consists of 40nm of Au on 5nm of Ti. A 10nm thick Al_2O_3 film was directly grown via atomic layer deposition (ALD) at $90°C$ as dielectric layer on the active device area. Source/drain electrodes were patterned onto Al_2O_3 layer via an electron-beam lithography step followed by a Ti/Au (5 nm/25nm) deposition. The source/drain separation is 2.4μm for all the devices. Subsequently, a single-layer of CVD graphene, previously grown on a silicon substrate, was transferred onto the Al_2O_3 film. Extreme care was taken during this technological step. CVD graphene was initially detached from the silicon substrate by using a thick layer of PMMA, spincoated onto the graphene layer. The sample was then aligned to the graphene sheet: an objective lens (Mitutoyo BD Plan DP 5X/0.14) was employed to monitor the transfer process. Since the PMMA and graphene layer (assembly), after the separation from the silicon substrate, presented several folds, in order to bring the assembly closer to the sample, the latter was heated up to 140°C: in this way the PMMA layer became soft, started to adhere on the surface of the sample and the folds disappeared. Residual parts of PMMA were then eliminated by cooling down the sample to room temperature and by using acetone, thus leaving only the graphene layer onto the device. Only a small square of graphene sheet was patterned by e-beam lithography. The pattern of this photolithographic step was divided into two parts. The first one consisted in a little square around the gate fingers, using a small aperture of the e-beam (20μm), magnification of 1000X and a write field of 100μm; the second one consisted in a bigger square partially overlapped with the first one, using a bigger aperture (120μm), magnification of 250X and a write field of 400μm. These squares were patterned onto the oxide layers. After development, it was necessary to etch the sample in order to remove the graphene from all the regions excluding the little squares on the gate fingers. Reactive Ion etching (RIE) was used, with the following parameters: 0_2 pressure of 15Sccm, forward power of 30W, chamber pressure of 60mTorr for a time interval of 60 s.

After fabrication, the samples were characterized in DC and RF regimes. DC characterization of our GFETs was performed in order to obtain the transconductance curve (I_d vs V_{gs}) at different V_{ds} values (Fig. 2a). The I_d-V_{gs} trend is linear for $I_d<V_{dirac}$: this relation directly descends from the peculiar dispersion diagram of graphene. The I_d-V_{gs} curve allowed us to evaluate the static transconductance (g_m), whose value deeply influence the cut-off frequency. We found that g_m grows with V_{ds} and exhibits a maximum value at V_{gs}=0.8V and V_{ds} =1.5V (g_m= 9mS) for a GFET with gate length of 1μm. Such voltage values were chosen as the operating point for for subsequent RFcharacterization, aimed at at evaluating the RF performance of these novel devices, in terms of maximal cut-off frequency. The scattering parameters of the extrinsic device were measured by using a vector network analyzer (hp8510C). Electromagnetic simulation of open and short structures were employed for the de-embedding of the launching structures. Intrinsic device parameters so obtained allowed us to evaluate the short circuit current gain values (h_{21}) and to identify an equivalent circuit of the GFET. From the S-parameters shown

in Fig. 2b-c, it is possible to observe that S_{11} shows a mainly capacitive input impedance, since the gate is isolated from the graphene channel by the oxide. Instead, S_{22} evidences a resistive output impedance component (112 Ohm), almost constant in the RF regime, associated to the drain-source shunt conductance. By observing the h_{21} trend (Fig.3), we can notice that the device shows the typical behavior of a single-pole low-pass system (-20 dB/dec derivative) with a cutoff frequency of around 8GHz, notwithstanding the relatively long (1μm) gate length.

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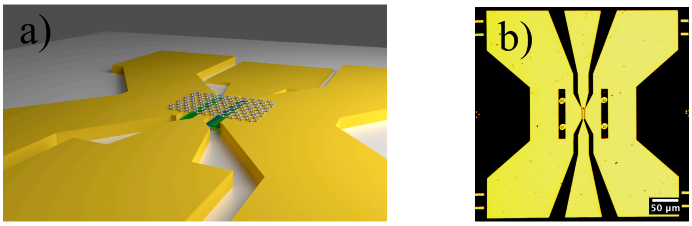

Figure 1: (a) Sketch of the devices under study. (b) Optical microscope photograph of the fabricated device.

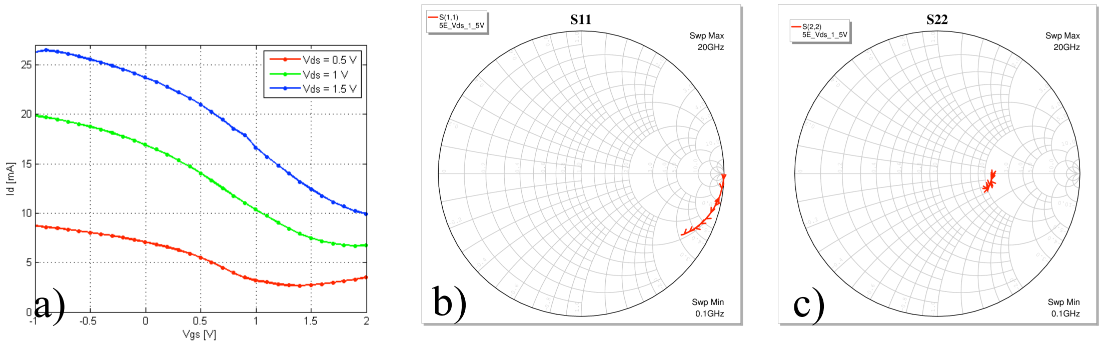

Figure 2: Measurements on 1μm-gate length device: (a) drain current as a function of the gate-source voltage, with drain-source voltage as a parameter; (b, c) scattering parameters S_{11} and S_{22} as a function of frequency.

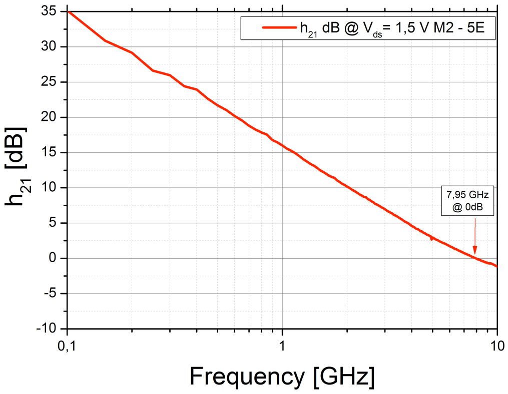

Figure 3: Small-signal short-circuit current gain ($|h21|_{dB}$) as a function of frequency at bias voltage V_{ds} =1.5V and V_{gs} = 0.8V (maximum DC transconductance).

K-band MMIC power amplifier based on a 3-stacked GaAS pHEMT device

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The microwave backhaul represents a key factor in determining cost and service quality of mobile communication systems. In a microwave radio, the Power Amplifier (PA) is one of the most demanding components, strongly affecting overall power consumption, hence the need of high efficiency architectures. Considering the ongoing trend towards an increased bandwidth and modulation complexity, also the PA linearity is becoming crucial. The frequency bands adopted for microwave backhaul are spread over the full microwave range, however, a significant number of systems work in the K-band [1]. While at lower frequencies the market is dominated by LDMOS and GaN technologies, capable to provide high output power, in this frequency range, PAs are usually realized in GaAs Microwave Monolithic Integrated Circuit (MMIC) technology. Being the power density of GaAs devices of the order of 0.5-1 W/mm, to achieve peak power levels around 2-10 W typical of backhaul applications specific combining strategies needs to be adopted. In this framework, a very promising solution is the stacked topology where two or more devices are series coupled forming an equivalent macro-device with enhanced breakdown voltage. Moreover, compared to more conventional combining methods, the stacked architecture reduces losses and allow increasing the bandwidth, as it increases the output impedance, thus mitigating output matching issues. The stacked configuration is already widely adopted in CMOS PA, while its application to GaAs PAs is becoming of interest only more recently [2-4]. Here we report the characterization results of a 3-stacked multiple common gate amplifier (Fig. 1) implemented in 0.15μm MMIC GaAs technology by TriQuint foundry. The authors have already discussed design and simulation results in [5]. CW characterization results in the 20–23 GHz range (Fig. 2) show early compression spots, negatively affecting the saturated output efficiency, which is lower than expected. Despite this, the amplifier performance are still satisfying and comparable to existent literature: saturated output power and efficiency in excess of 31.8 dBm and 27%, respectively, and gain higher than 9.5 dB in the whole bandwidth. To verify the stacked macro-device in absence of high-frequency effects, the same basic cell has been manufactured for low frequency (2–6 GHz) operation (Fig. 3). With output power in excess of 33 dBm the CW and load-pull characterization results on this module (Fig. 4) confirmed the potential of the staked topology and its equivalence with a single device. At 4 GHz (Fig. 5) the presence of early compression spots similar to what experienced in K-band in case of output mismatch, suggest that the issues encountered at high frequency are due to the impact of process variability and inaccuracy of the large-signal device model on output matching.

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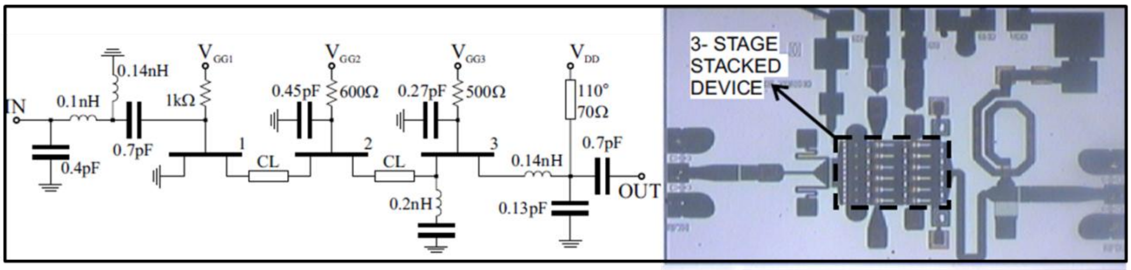

Figure 1: Scheme and microscope picture of the 3-staked PA: the extreme layout compactness of the 3-stacked cell suggests that it can be effectively exploited as macro-device in more complex monolithic architectures.

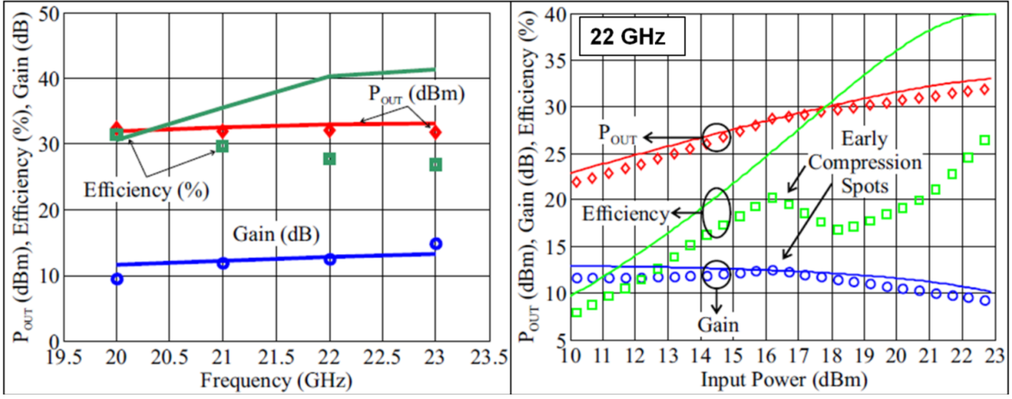

Figure 2: CW characterization results.

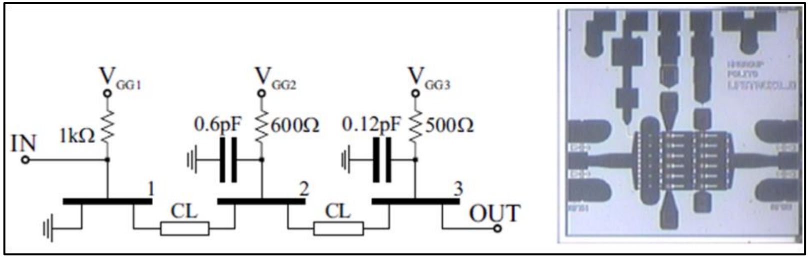

Figure 3: Scheme and microscope picture of the low-frequency 3-stacked PA.

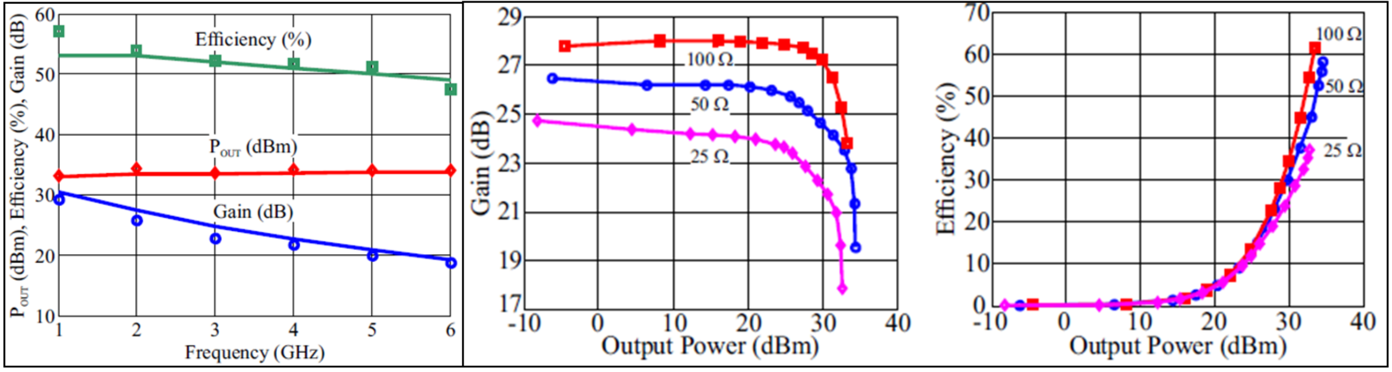

Figure 4: CW and 2 GHz load-pull characterization result on the low-frequency 3-staked PA.

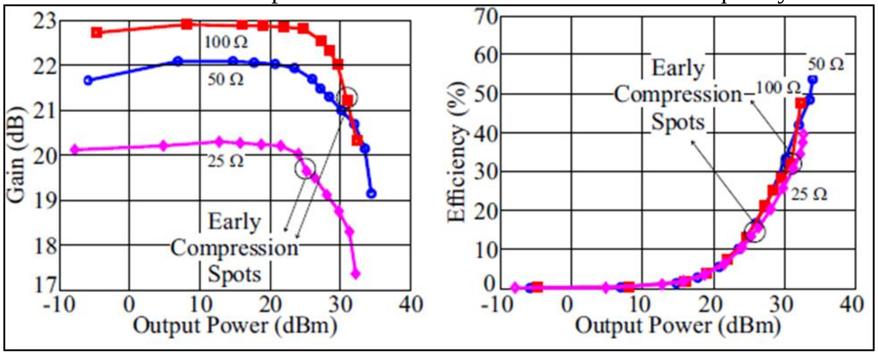

Figure 5: 4 GHz load-pull characterization results of the low-frequency 3-stacked PA.

Self-Interference Cancellation for Free-Flow Road-Tolling Collection Transceivers at 5.8 GHz

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This paper describes the architecture, the design techniques and technologies suitable at the development of a radio hardware interface for a road-side equipment (RSE) compliant with the requirements of electronic toll collection (ETC) for vehicular applications based on the EN300674-1 standard, [1].

This specific application considers an array of RSEs installed on gates across the roadways operating in frequency carrier diversity and sending the same synchronized down-link message. The information are exchanged with an on-board unit (OBU) installed on cars moving through the gate, cfr. Fig. 1. In the figure is reported the simplified picture of multi-lane free-flow (barrier-free) ETC scenario, where each RSE is supposed to communicate with the same car (i.e. with the same OBU). Being the OBU a semi-passive transponder, [2], the transceiver (cfr. Fig. 2) implements a full-duplex channel radio access and features a digital-IF down-converter scheme at receiver to deal with different profiles, communication modes, carrier frequencies as well as channels.

The communication between RSEs and OBUs imposes several issue for a radio-frequency architecture design point of view, the main of them consists in the self-interference which desensitize the RSE receiver [3]. This issue is even more severe when considering the RSE as a part of an array of RSEs transmitting 39 dBm of peak power and operating in relative close proximity (approximately 3.75 m), at one out four of the carrier frequency available from the regulatory. Thus the presence of strong signals at the receiver during the reception of the OBU signal, requires that at least the self-interference would be minimized. This is achieved including a transmitter leakage canceller at the front-end of the RSE transceiver Fig. 3, [4]. Its operation mode is effective and in principle quite simple. It samples the transmitter carrier and operates on it a phase rotation and a proper magnitude scale, then re-couples it to cancel the self-interferer at the receiver input. This procedure is proven (cfr. Fig. 4) to improve to about 70 dB the effective isolation between transmitter and receiver, to which corresponds a signal-to-noise ratio improvement up to 38 dB. The effective cancellation of the self-interference makes the requirement on the side RSEs carrier interference less stringent.

This cooperative RSE down-link operation relies on a complex digital-IF receiver (cfr. Fig. 5). For the multi-lane free-flow ETC applications under consideration, the up-link signal spectrum is schematically depicted in Fig. 6. In the figure we recognize the ASK back-scatted signal in response to two different carriers incident on the same OBU. The frequency planning is such that only the upper and the lower side bands respectively for the higher and the lower carriers results unaffected from the carrier over-imposing, and thus represents the useful band to be detected. This selection is achieved with the complex digital-IF down-converter which is capable to shift the IF spectrum toward either the negative or the positive frequency, respectively for the higher of lower carrier. The Fig. 6 (left) reports the schematic spectra during the down conversion at RSE2 (i.e. higher frequency carrier). An example of the measured spectrum after the first analog down-conversion is reported in the Fig. 6 (right), where it is possible to observe the right-side band of the up-link signal about the higher carrier and also the lower one component corrupted by the lower carrier.

The talks provides a detailed discussion of the above highlighted topics giving an inside view of the transceiver design challenges, as well as laboratory experimental result and on-field test carried in the realistic trial field test provided by Autostrade per l’Italia SpA.

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Figures and captions

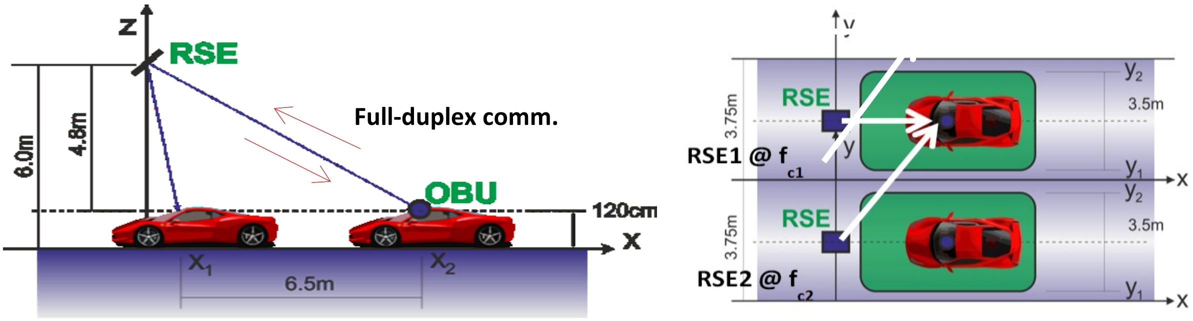

Fig. 1: Layout configuration for of the free-flow ETC system; downlink between two RSEs and same OBU

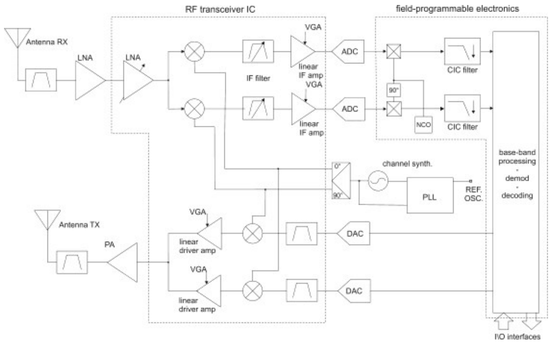

Fig. 2: Architecture of the 5.8 GHz full-duplex transceiver

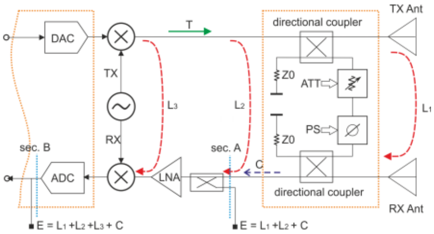

Fig. 3: Analog active canceller architecture

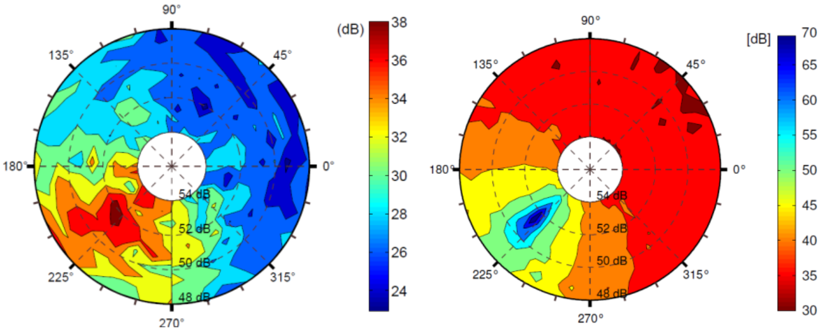

Fig. 4: Experimental validation of the canceller performance (left) and the related SNR improvement (right)

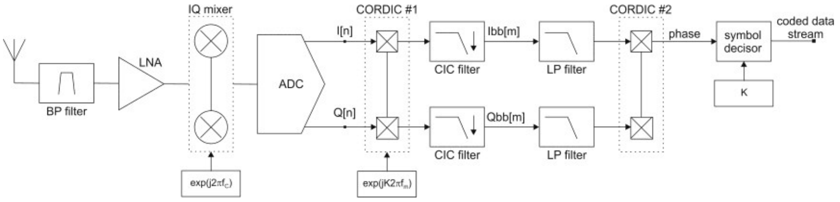

Fig. 5:schematic representation of the receiver chain with the digital-IF section

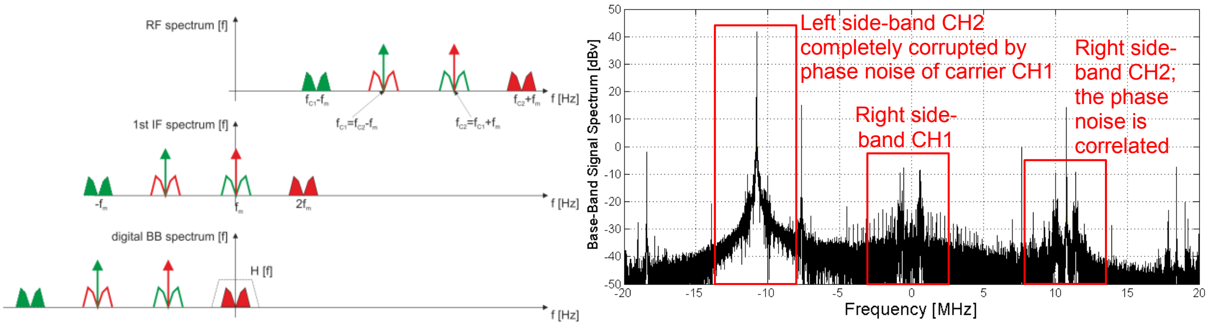

Fig. 6: Schematic representation of the up-link spectrum at different section of the receiver for multi-line multi-carrier mode (left); measured spectrum at firs down-conversion for carrier #2 (right)

Single-chip front-end for T/R modules in GaN technology

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The present contribution summarizes the activities performed towards the realization of a Single-Chip Front-End (SCFE) operating in C Band, integrating the High Power, Low Noise amplification and switching functionalities to be provided in modern T/R modules’ Front-Ends for space Synthetic Aperture Radar (SAR) applications. Evolution of such systems in the next years can be envisaged on the basis of the scenario identified by the different users’ needs. In fact, Earth monitoring is receiving more and more attention on society needs and science/research thus demanding services involving different operating bandwidths. To improve system features, it is necessary to increase output power, while simultaneously maintaining a small antenna. Such a demanding constraint implies a change in the electronic component technology. GaN is an almost ideal semiconductor for these applications. Compared to GaAs its breakdown electric field is about 10 times and the power density is about one order of magnitude. In the specific context of a T/R Module, GaN may be efficiently applied on Transmitting and Receiving sections [2]: the high power density associated with GaN devices will allow a higher RF output power and hence a smaller size for the High Power Amplifier. Further, GaN devices have been shown to have similar characteristics in terms of Noise Figure compared to GaAs. Higher breakdown and the capability to withstand higher voltages, translates into the possibility to eliminate the T/R module limiter [2]. All of these reasons motivate the efforts of the SCFE project. Its design of SCFE has been tailored for two technologies, i.e. the UMS GH25-10 and the SLX SXGH05L. The preliminary steps were the design of the LNA, HPA and the Higher Power T/R switch and the resulting parts have been interconnected to form the SCFE. The two layouts of the module (one for each technology) are shown in Figure 1 and 2. For the Tx-mode the performance is as follow: for both chips the input match is better than 10 dB, the small-signal gain is >46 dB (UMS) and >38 dB (SLX). The output power is 40.4 W with a PAE of 36.3% for UMS. For SLX output power is 45.9 dBm and the PAE is 27% at 4 dB compression (Figure 3 – UMS, Figure 4 – SLX, Tx performance). Regarding Rx-mode performance, both chips are featured by a 36 dB small-signal gain. Noise figure firmly remains below 2.5 dB for both chips, accounting also for the insertion losses of the input T/R switch. Input matching is better than 10 dB for both designs as well as the output matching, always better than 15 dB (Figure 5 – UMS, Figure 6 – SLX, Rx performance). The resulting chips are featured by very good performance in term of output power (>40 W), noise figure (<2.5 dB) and remarkable efficiency levels (>36% - UMS and >27% - SLX). To the authors’ knowledge, this combination of performance in a SFCE represent the state-of-the-art for T/R modules.

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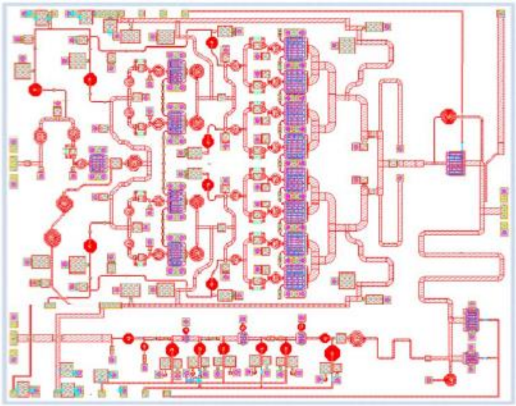

Figure 1: UMS SCFE Layout. MMIC size 6.9x5.4mm^2.

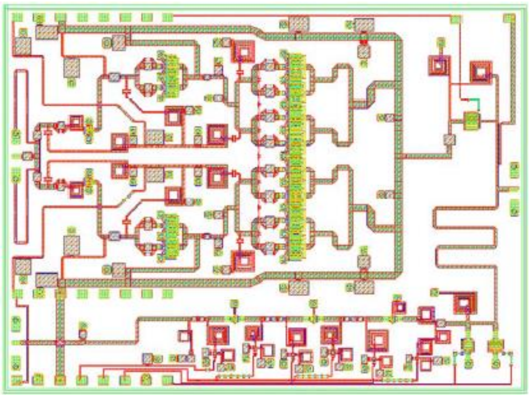

Figure 2: SLX SCFE Layout. MMIC size 7.3x5.4mm^2

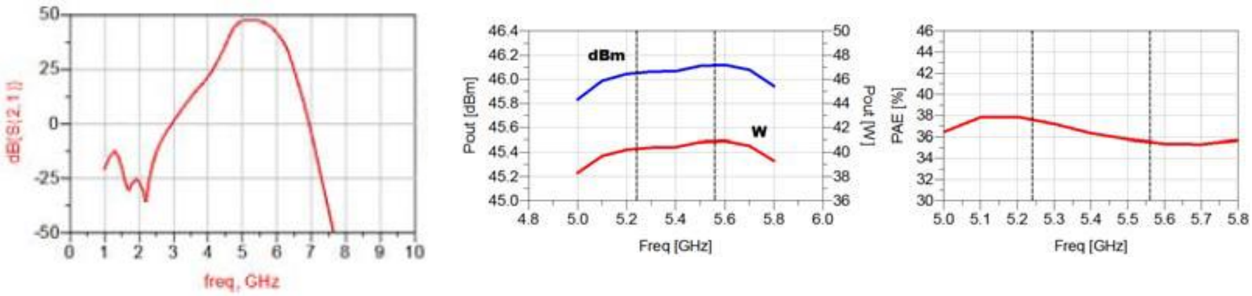

Figure 3: UMS SCFE performance Tx mode.

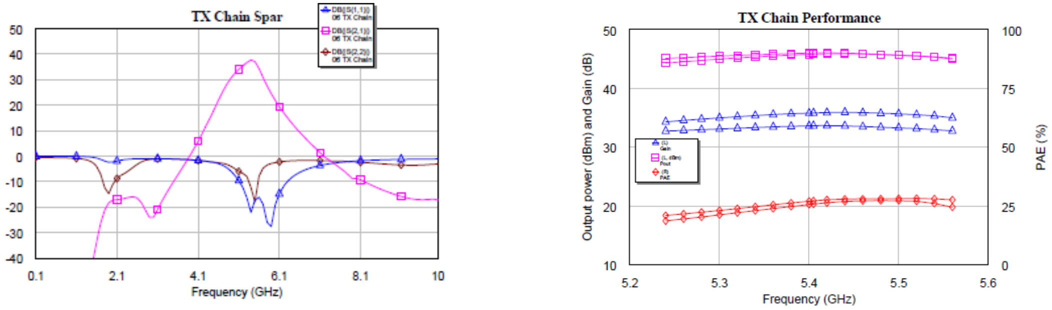

Figure 4: SLX SCFE performance Tx mode.

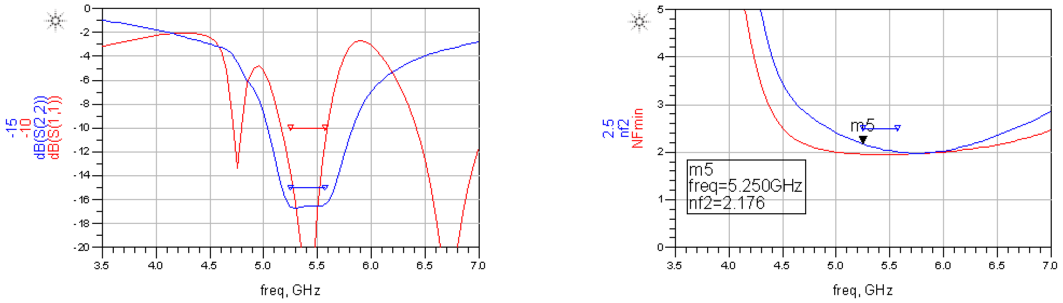

Figure 5: UMS SCFE performance Rx mode.

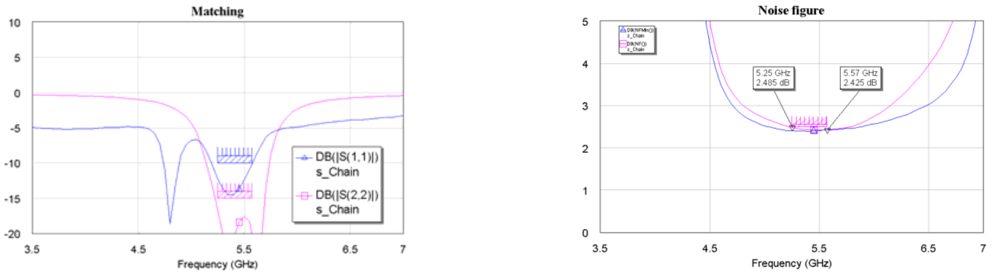

Figure 6: SLX SCFE performance Rx mode

Terahertz CMOS Integrated Image Detectors

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We present a new semiconductor device, CMOS compatible, operating at room temperature, for the rectification of signal in direct conversion up to the terahertz. The rectifying device can be obtained introducing some simple modifications of the charge storage well in conventional CMOS APS devices, making the proposed solution easy to integrate with existing imaging systems [1]. No need of scaling toward very scaled and costly technological node is required, since the CMOS only provides the necessary integrated readout electronics.
The structure is directly integrated with a nanometric metallic whisker, which represents one of the edges of a truncated conical helix extruded from a planar spiral capable to receive the Terahertz radiation. The semiconductor substrate that constitutes the antenna ground plane. With the rectifying devices constitute a rectenna structure.
On-wafer measurements of RF characteristics of the designed rectifying junction are reported and discussed.

In Fig. 1 a) the structure of the rectenna and its connection with the photodetector is presented. Simulations showed that a Field Enhancement up tp 40.000 can be obtained, see Fig.2 [2, 3, 4]. The structure is designed as a combination of an antenna fabricated on the surface of the chip with a rectifying junction capable to produces the direct conversion of terahertz electromagnetic field into DC current. Different semiconductor devices can be used for this purpose, e.g. Schottky diodes, MIM diodes, low barriers junctions. Nevertheless, the necessity to adopt an approach as close as possible to the technology of CMOS photodetectors, induces to use a metal/oxide/semiconductor (MIS) structure as it may take the advantage of gate oxide already present in the detector structure. The rectifying structure presented here is realized by a double barrier formed by the metal of the whisker [5], chosen with working function similar to an n+ doped semiconductor, a p+ doped surface layer and by the semiconductor storage well.

Numerical simulations of the semiconductor device, performed by means of Synopsis Sentaurus TCAD tools, strictly confirm the rectifying capability.

We developed a test structure, Fig.3, to verify the rectification properties of the detector. The test structure does not include the antenna and is designed for tests at frequencies below the THz range. The test structure is realized with minor changes from a standard configuration of a CMOS photo-detector using Aptina-ON Semiconductor 0.15µm technology node.

Measurements where performed in the range 1-40 GHz, on several samples with different parameters of the *p*-type doping implantation.

Errore. L'origine riferimento non è stata trovata.4 reports the rectified current measured versus the RF power applied to the signal pad at 1 and 40 GHz. Numerical simulations showed that the rectification process, experimentally verified only up to 40 GHz, is also effective up to 1THz, showing in particular one pole behavior, with a cut-off frequency of 120GHz. Experiments and simulations, combined, lead to the evaluation of NEP at 1 THz of $51.10^{-12} W/\sqrt{Hz}$.

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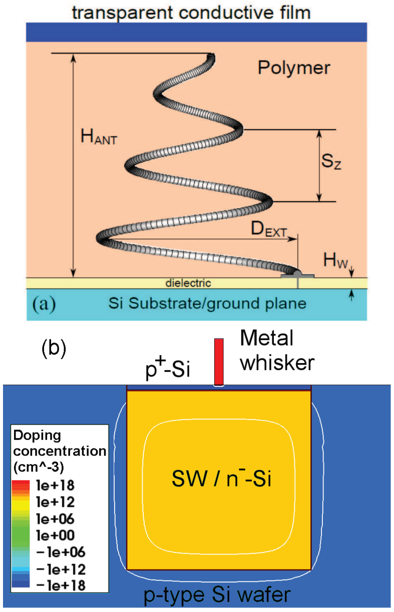

Fig. 1. (a) Schematics of the rectenna geometry. (b) Schematic front view of the antenna pad and of the metallic whisker facing the storage well.

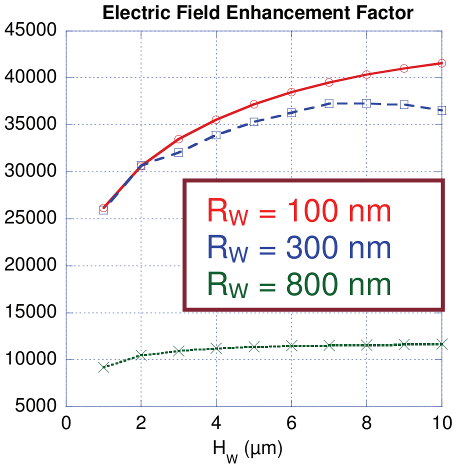

Fig. 2.The ElectrciField enhacement factor obtained from simulations on 3D helix tapered antenna. Hw and Rw are respectively the whisker heights and diameters.

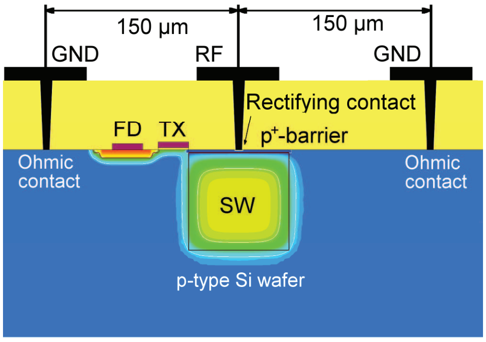

Fig. 3. A schematic description of the test structure. Dimensions of the RF pads and of the SW are not in scale.

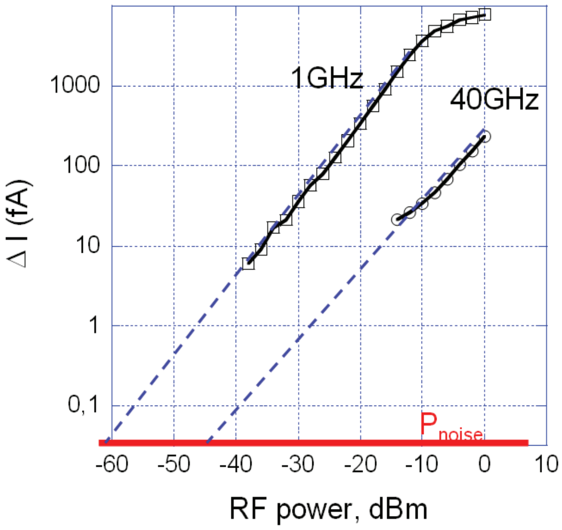

Figure 4. Rectified current versus applied power for the twofrequency, respectively 1 GHz and 40GHz.

The rectified current is compared with the noise level, 200 e/sec, expected in the detector storage well.

A simple method for measuring OLEDs efficiency

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External quantum efficiency (EQE) of organic light emitting diodes (OLEDs) is among the most important parameters for devices assessment and for comparing OLEDs performance. The EQE is the ratio of the total number of photons emitted by the OLED in all directions to the number of electrons injected.

The key point is to measure the total optical power P_{TOTAL} emitted by the OLED in the half space (i.e. waveguided light is not considered), taking into account that an LED is a polychromatic light source with a certain spatial emission pattern. To measure P_{TOTAL} a large area calibrated Si photodiode (PD) of known responsivity (W/A) placed in contact with the OLED surface can be used [1]. This requires the measurement of the PD photocurrent, together with the OLED emission spectrum to calculate the "equivalent" responsivity of the PD. The luminous efficiency (cd/A) and luminous power efficiency (lm/W) can be calculated using the photopic visibility curve and the OLED emission spectrum [2]. A calibrated Si PD is meant to be used for normal incidence of the light beam to be measured. The reflectance of the PD glass window increases for obliquely incident rays and with the PD placed in contact with the OLED surface [1] one measures an emitted optical power that is less than P_{TOTAL} but more than the power emitted by the OLED in the normal direction.

Here we present a simple geometrical modification of this method, where the PD with radius r_{PD} is placed on axis at a distance d_{PD} from the OLED with radius r_{OLED}, as shown in Fig. 1, where a radial symmetry is assumed. If $d_{PD} >> (r_{PD}\ , r_{OLED}\ )$, the PD "sees" the OLED as a point source and, taking into account the OLED spatial emission pattern I(θ), the power P_{PD} impinging on the PD area is simply related to P_{TOTAL} by:

$$f = \frac{P_{PD}}{P_{TOTAL}} = \frac{\int_0^{\theta_{PD}} I(\theta)d\theta}{\int_0^{\pi/2} I(\theta)d\theta} = \sin^2\left(arctg\,\frac{r_{PD}}{d_{PD}}\right) \qquad (1)$$

where the last equality holds for a Lambertian source $I(\theta)=I_0\cos\theta$. This is a good approximation for a bilayer AlQ3 based OLED with negligible microcavity effects [3]. If the radiation pattern I(θ) is measured in advance the method can be extended to any LED source. To assess the minimum distance d_{DP} for the method validity, we measured P_{PD} vs. voltage for a 3 mm^2 AlQ3-based OLED using a calibrated Si PD (NEWPORT 808-UV with 100 mm^2 area, i.e. r_{PD} = 5.6 mm) varying d_{PD} from 6 cm to 12 cm, as shown in Fig. 2. P_{TOTAL} calculated using the correction factors f given by (1) and the corresponding luminance vs. voltage are shown in Fig. 3 including d_{DP}=0 cm i.e. the PD placed in contact with the OLED surface. Independently from d_{PD}, it can be noticed that P_{TOTAL} values are the same. As expected, with the PD placed in contact with the OLED surface the measured power is about 18% less than P_{TOTAL} above.

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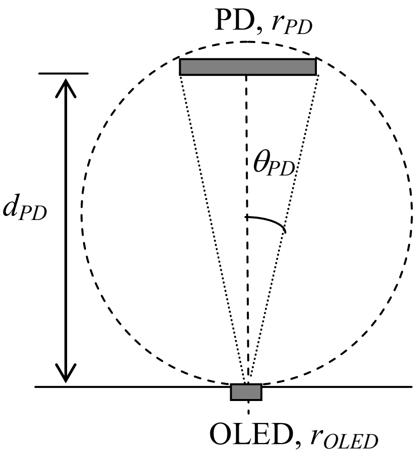

Fig. 1: Geometry of the measurement set-up.

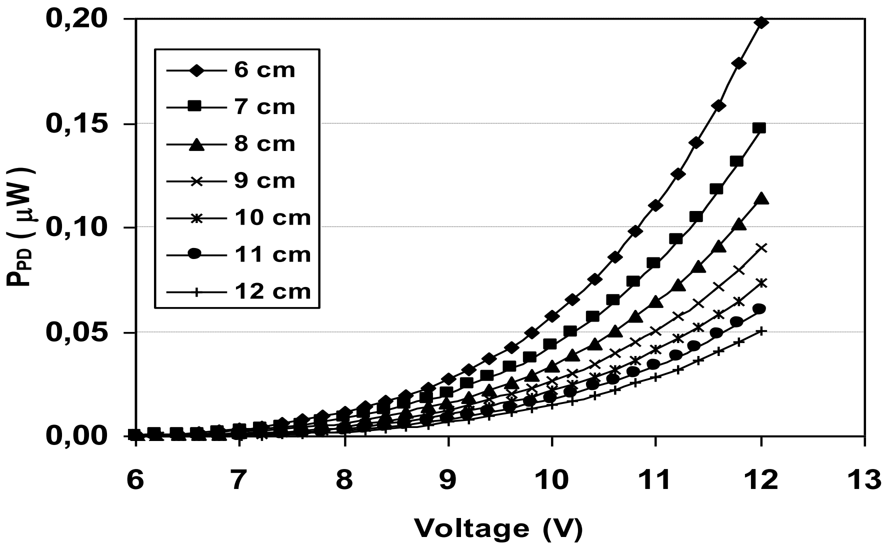

Fig. 2: P_{PD} vs. voltage with variable d_{PD}.

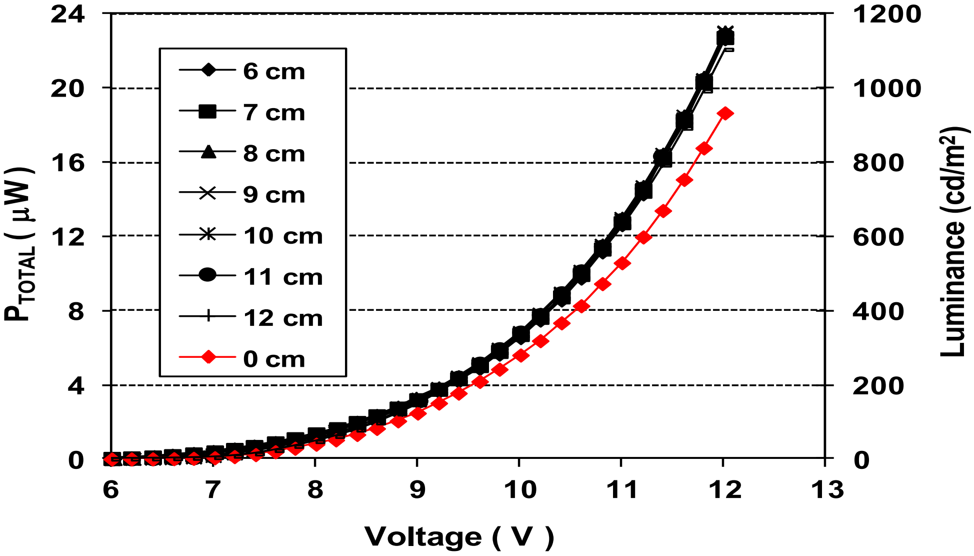

Fig. 3: P_{TOTAL}, calculated using the correction factor f, and the corresponding luminance vs. voltage with variable d_{PD}, including d_{PD}=0 cm.

APPLICATION OF FBG SENSORS TO STRAIN AND TEMPERATURE MONITORING OF THE CMS UNDERGROUND DETECTOR AT THE CERN LABORATORIES

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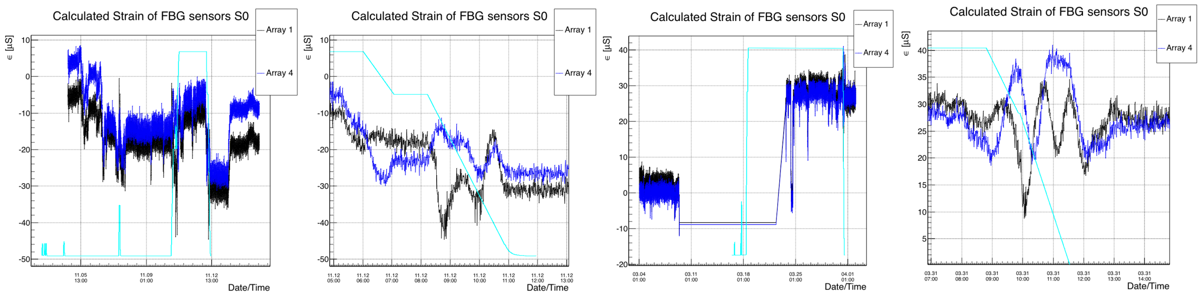
Recent results of structural and thermal monitoring of the Compact Muon Solenoid (CMS) Experiment at the European Organization for Nuclear Research (CERN) laboratories will be reported. The measurements are carried out by means of a large number of Fiber Bragg Grating (FBG) sensor arrays installed in the CMS underground detector. In particular, we will report data concerning temperature and strain measurements recorded during CMS maintenance interventions in last period (LS1) and first period (Run2) of Large Hadrons Collider (LHC) collisions starting in April 2015.

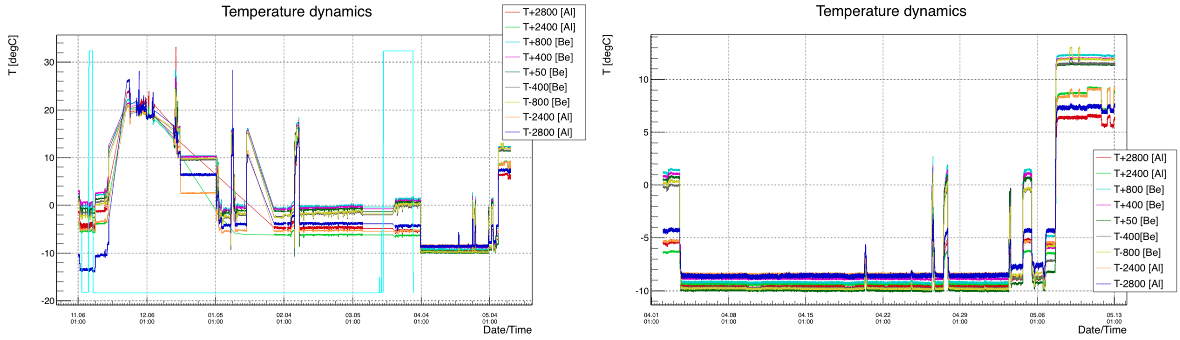
Being spectrally encoded, the FBG sensors are insensible to EM interference, intensity modulation of the optical carrier and broadband-radiation-induced losses. All these characteristics allow to perform long distance punctual sensing systems, capable to operate in harsh environments like the underground experimental facilities at CERN. Radiation immunity represents the most important specification required to a monitoring system operating in a High Energy Physics (HEP) environment. CMS-CERN needs are: no EM interference with particle detectors, low complexity layout, multiplexing and multi-parameters measurement capabilities and radiation hardness. Nuclear radiation effects on optical materials and photonic devices have been studied since several decades [1,2]. Ionizing radiation, mainly, produces wavelength dependent radiation-induced attenuation in optical fibers. Hence, fibre optic monitoring FBG based system represents the ideal solution to achieve a reliable and accurate sensing system to be used 24/7 in the harsh environment at CMS. Based on these technical specifications, a fiber optic strain and temperature monitoring system was designed and developed by our research group.

In 2009 we installed first configuration of FBG based monitoring systems in the underground site of CMS experiment. It was gradually increased up to 200 temperature and strain sensors, running 24/7 for 3 years during LHC collisions, without any interference with CMS operating conditions [3]. Since February 2013 until March 2015 the LHC has been stopped in order to allow technical interventions and upgrade of the machine and experiments. During this period we expanded our FBG monitoring system. Now we have nearly one thousand FBG sensors installed and operational, covering the CMS experiment from the outer to the most inner part. In particular we installed a new FBGs strain (temperature compensated) monitoring system on the new Central Beam Pipe of the CMS experiment to monitor on-line unintentional and unpredictable mechanical deformations. From this monitoring system we have detailed measurements for any deformation induced on central beam pipe by any motion in the CMS detector due to element displacement or to magnetic field induced deformations. Preliminary data collected so far showed the stability of CMS central Beam Pipe and the high level of sensitivity and reliability of this monitoring system (see Figure 1 and 2). This monitoring system will also secure the measurement of the temperature distribution along the CMS central beam pipe during maintenance and operation phases. In addition, it will help to improve the safe operation of future CMS opening/closing activities and beam pipe manipulations. This innovative, FBG based, monitoring system will be a milestone for any future beam pipe monitoring in High Energy Physics domain.



(a) (b) (c) (d)

Figure 1. Strain behaviour on the central part of the pipe during the B-field test performed in November 2014 (a,b) and in March 2015 (c,d). Figures (b) and (d) are focused on the strain acting on the beam pipe during the rumping down of the B-field; the time windows is of 8h. Straight lines represent intervals during which the DAQ was off for technical reasons. The cyano line represent the B-field behaviour, whose maximum is at 3.8T.



(a) (b)

Figure 2. Temperature dynamic of the beam pipe. In Figure (a) the time windows goes from 2014/11/06 to 2015/05/13, while Figure (b) is focused during the first period of LHC operations, from 2015/04/01 to 2015/05/13. Straight lines represent intervals during which the DAQ was off for technical reasons. The cyano line represent the B-field behaviour, whose maximum is at 3.8T.

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Charge instabilities in electro-thermally stressed blue InGaN laser diodes

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Optoelectronic devices based on Gallium Nitride are rapidly emerging as excellent light sources for use in the lighting field, for optical data storage, for projection systems, and for optical signal transmission in the blue-green optical band. The creation of alloys containing indium allows for the tuning of the peak wavelength, but still poses problems of reliability and lifetime in typical operating conditions. The devices under test are commercially-available blue InGaN-based Laser Diodes (LDs), with a typical output power of 100mW and a peak wavelength of 405nm at the nominal operating current of 120mA. We have performed stress tests at various currents (0, 20, 40, 60, 80, 100 mA) and temperatures (30, 45, 60, 75 °C), and at each step we measured the main characteristics of the device: i) the voltage - current relationship, to obtain information on the variation of the conductivity of the devices; ii) the output optical power at various bias currents, from which we calculated the threshold current and slope efficiency; iii) the capacitance and conductance of the devices as a function of frequency and applied voltage, in order to understand how the charge distribution changes inside the LD.

The analysis of the stress kinetics indicates the presence of two different mechanisms (Fig. 1 and 2), that induce an initial decrease and a subsequent increase in threshold current.

In the initial phase of the stress experiment, we have measured a significant improvement of the optical properties of the devices, mostly consisting in a decrease in threshold current. This variation exhibits almost no dependence on bias current, and is completely blocked when no electrons flow through the device and only temperature is applied. Moreover, the effect is strongly promoted at higher temperatures (see Figure 3, which reports the results of the first hours at different temperatures). Based on previous literature reports [1,2], we tentatively attribute this mechanism to the activation of the p-type dopant during the first steps of stress, induced by the flow of a high density of carriers within the active region of the devices. Figure 4 shows that there exists a good correlation between various quantities that are influenced by an increased magnesium activation: i) the threshold current decrease; ii) the variation of the forward voltage of the laser diode; iii) the drop of the conductance. The fact that stress induces an increase in the charge profile can be confirmed also by analyzing the changes of the capacitance when different voltages are applied. In the inset of Fig. 5 we can see a clear increment of the carriers in coincidence with what we found in Fig. 3.

The second part of the degradation kinetics is dominated by an increase in the threshold current (Fig. 1 and 2). Based on previous literature reports [3], this process is consistent with the generation of defects, that act as non-radiative recombination centers and increase the leakage current by providing additional tunneling/recombination paths (see Fig. 6).

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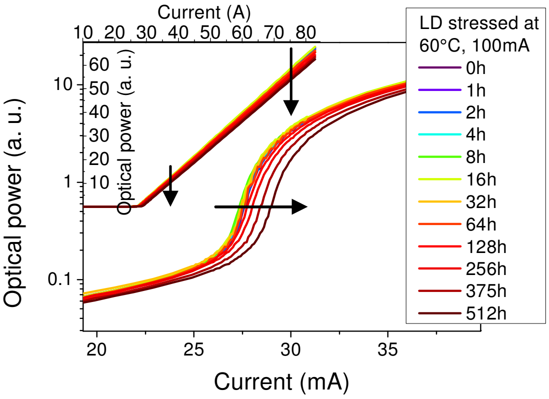

Fig. 1: Output optical power versus bias current after various stress steps at 60°C, 100mA.

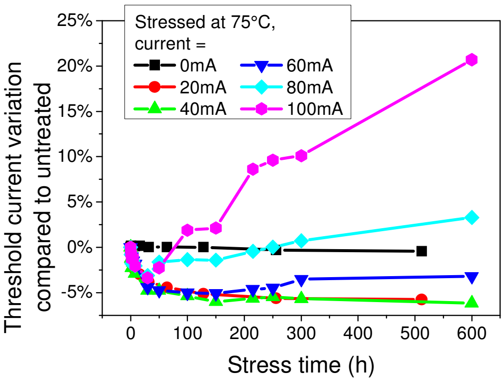

Fig. 2:Effect of stress current on threshold current of LD stressed at 75°C.

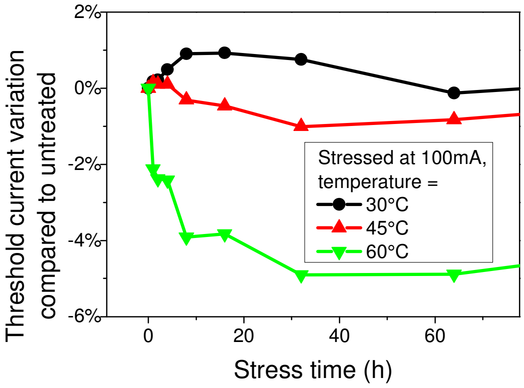

Fig. 3: Variation of the threshold current during the first stress steps at 100mA and various temperatures.

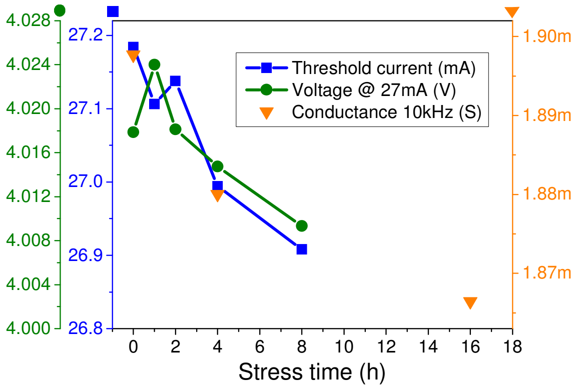

Fig. 4: Correlation between the variation of threshold current, forward voltage and conductance at 2.9V. Device stressed at 60°C, 100mA

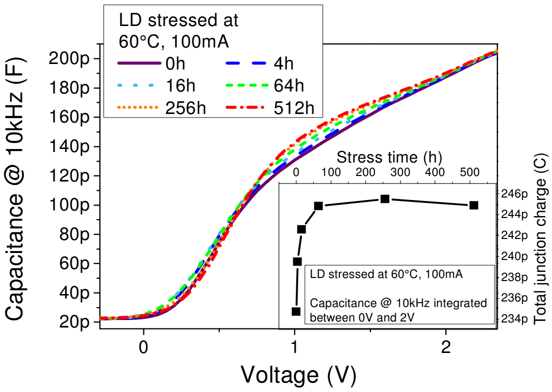

Fig. 5: Capacitance and junction charge variation after stress at 60°C, 100mA.

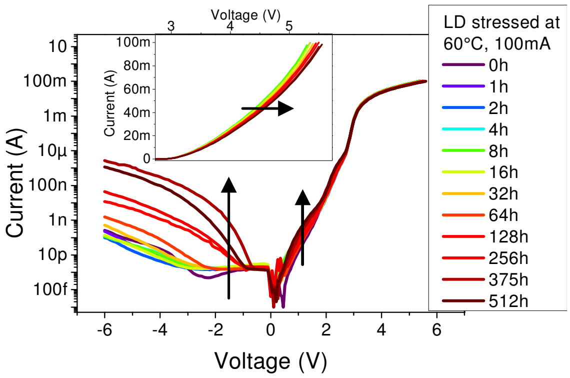

Fig. 6: Current-voltage relationship of a Laser Diode stressed at 60°C, 100mA.

Development of High Performance Photovoltaics for Indoor Light Harvesting

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Photovoltaics is a premier renewable energy source. The great majority of the development of photovoltaic technologies is focused on operation in the outdoors, i.e. under standard test conditions (STC: AM1.5G, 1000 W/m^2, 25 °C). However, increased attention is arising in the quest for finding power sources that can deliver efficient harvesting of energy in indoor ambient conditions. The applications are far-ranging, especially related to internet of things, domotics and building management systems [1]. The uptake of energy harvesting devices is related to the successful development of effective power sources that can be used indoors generating enough energy to drive electronic devices, such as wireless sensors, in buildings. One of the prime candidates is represented by photovoltaic cells, especially in their thin flexible form for more seamless integration. In order for its wide adoption, photovoltaics needs to perform under artificial lighting.

Here we compare the power output of PV cells of the dye sensitized type we fabricated and customized for indoor use with commercial samples of solar cells (crystalline and amorphous silicon PV) measured under artificial light, i.e. compact fluorescent lamps (CFLs) and light-emitting diode (LED) lighting.

Dye sensitized solar cells (DSSCs) have been reported to deliver very high performance in indoor conditions from industry but reports on their customization for artificial light environments are not present in the literature. We show (see Figure 1) that the customization of flexible DSCs, by formulating ad-hoc less-concentrated more-transparent electrolytes, enabled these devices to outperform all others, providing average power densities of 8.0 µW/cm^2 and 12.4% efficiencies (more than quadruple compared to those measured at 1 sun) under 200 lux CFL, and 6.6 µW/cm^2 and 10% efficiency under 200 lux LED illumination. In comparison poly-Si cells with 15% outdoor efficiency delivered at 200 lux under CFL only 2.8 µW/cm^2 power density (and an efficiency of 4.4%), and a-Si specifically designed for indoors, gave 5.9 µW/cm^2 and 9.2% efficiency under the same CFL conditions (and 7.5% under LED). Thus our customized DSCs surpass the performance of commercial photovoltaics under indoor lighting [2].

Finally, we will also summarize what kind of electronic devices (e.g. wireless sensors, active ID tags, etc.) can be powered, depending on the dimensions of the photovoltaic module to be integrated in the electronic system and the operation cycle of these sensing devices.

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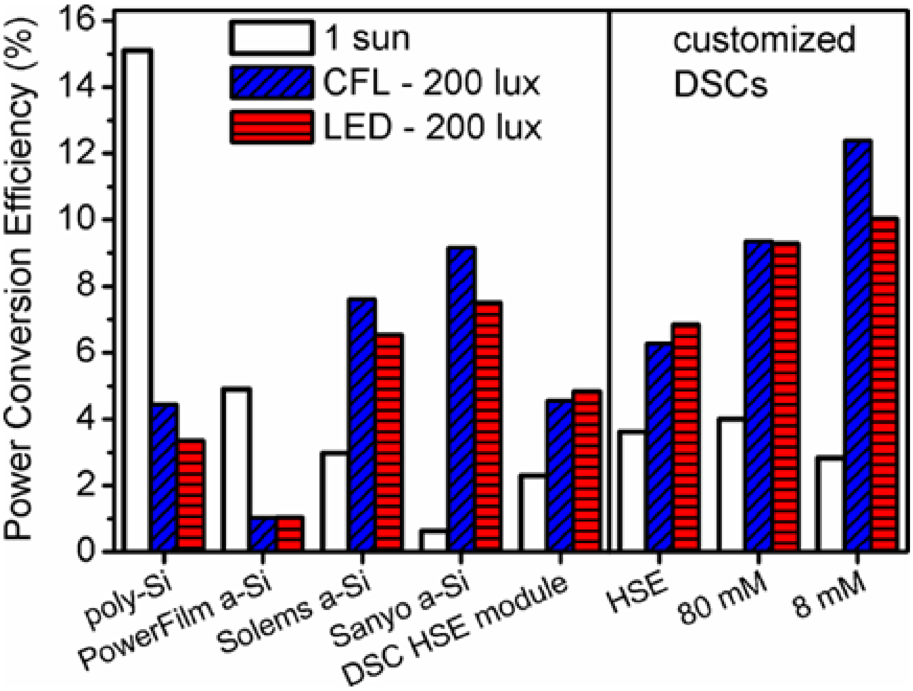

Figure 1: Power conversion efficiency (PCE) of the investigated photovoltaic devices under CFL (blue bars with diagonal lines) and LED (red bars with horizontal lines) light sources at 200 lux illuminance, compared to values obtained under sun simulator at 1 sun illumination (white bars). The same data referring to small back-illuminated DSCs with the standard electrolyte, i.e. HSE, and customized electrolytes (80 and 8 mM iodine respectively) are also reported. As can be noted, under indoor lighting, our customized dye solar cells deliver the highest efficiencies [2].

Electro-optical characterization of highly efficient Dye-Sensitized solar cells

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Nowadays, a growing demand for free and clean energy requires the study and the development of new low-cost solar photovoltaic (PV) cells. Among them, Dye Sensitized Solar Cells (DSSCs) based on ruthenium complexes as sensitizers are assuming a great importance [1]. The DSSCs under study are composed placing in succession a transparent conductive glass on which is screen-printed a mesoporous TiO_2 thin film sensitized by a ruthenium based dye (N719), an electrolytic solution containing a redox couple (I^-/I_3^-) and another conductive glass covered by a thin transparent catalyst platinum film [2,3]. In this work, we have measured the main photoelectrochemical parameters of the above mentioned DSSCs at different irradiance levels, incident wavelengths, temperatures and hours of light soaking. A first characterization was performed with narrow-band light sources at varying incident wavelengths using a Newport Oriel solar light simulator and ten pass-band optical filters with a bandwidth of 40 nm and central values between 400 and 850 nm (see Fig. 1). The obtained results show a maximum conversion efficiency around 11-12% in the range within 540 and 550 nm (see Fig. 2).

A full characterization with the solar simulator at different irradiance levels (up to 1000 W/m^2) was carried out. For all the available samples, we have obtained the I-V characteristic curves at different irradiation intensities, even in the dark. The I-V curves showed a rectangular-shaped form, hence leading to a high fill factor. In addition, the open circuit voltage V_{oc} increases with the irradiance. The efficiency does not vary within the range 600-1000 W/m^2, slightly diminishing for lower irradiance values. Furthermore, a characterization with white light sources at five hours of light soaking was performed at a fixed irradiance value of 1000 W/m^2 and at 15°C temperature. Our results show that the short circuit current density J_{sc}, the open circuit voltage V_{oc} and the conversion efficiency η increase with the hours of light soaking (Fig. 3).

The above mentioned parameters increase in an exponential-like behavior, with a saturation reached after about five hours of light soaking. The J-V characteristic curves at several temperatures in the range from 15°C to 70°C were measured (Fig. 4). J_{sc}, V_{oc} and η decrease almost linearly with the temperature, up to 65°C at least. Further studies are underway to obtain a more detailed explanation of the physical and chemical features that influence the above-described trends.

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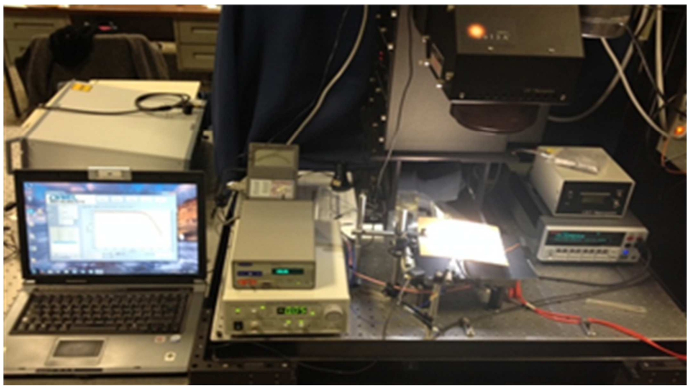

Figure 1: Experimental set-up for the electro-optical characterization.

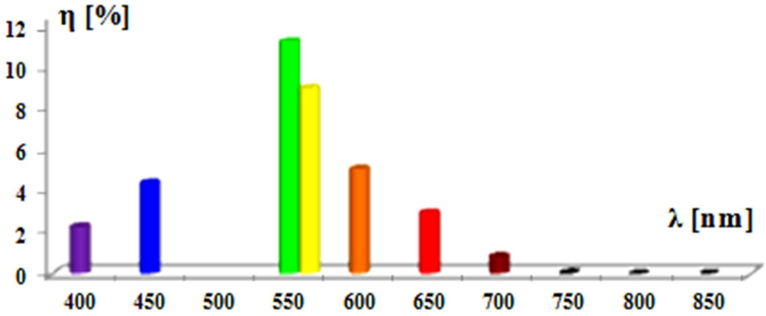

Figure 2: Efficiency measured at diverse wavelengths.

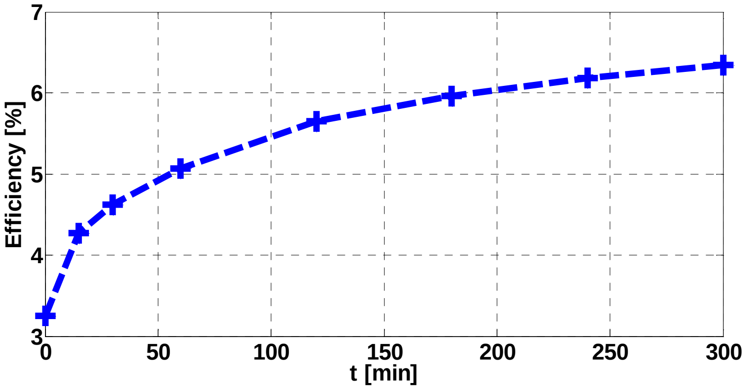

Figure 3: Efficiency measured at five hours of light soaking.

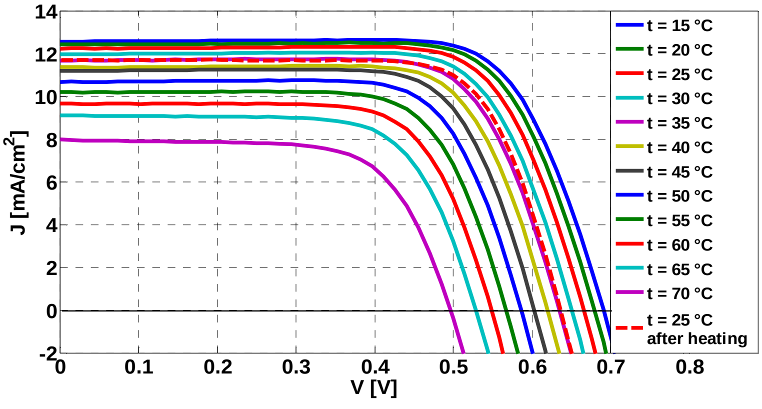

Figure 4: Characteristic J-V curves at several temperatures.

Fabrication of graphene ruthenium-complex heterostructures

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The aim of this study is to understand the photoresponse of a Ruthenium-complex/graphene heterostructure. Early work demonstrated that light detection by graphene field effect devices was enhanced by dropcasting Ruthenium Complex molecules [1]. Here we proposed to fabricate a new class of devices where the Ruthenium-complex molecules are embedded between two layer of CVD monolayer graphene.

Due to the atomic thickness of graphene (atomic monolayer) and the resulting small optical absorption together with short recombination times, efficient photodetection is not possible with bare graphene. This issue can be addressed using different approaches. One way is to enhance the interaction length between the light and the graphene by the use of an optical cavity. Another way is to open a bandgap, e.g. by patterning the graphene into nanoribbons and therefore increasing the recombination time. A third way is the use of so called heterostructures. In this case other materials are used to harvest the light while graphene is only used because of its electrical properties [2].

In this work a graphene-Ruthenium-complex heterostructure is fabricated. Ruthenium molecules were synthesized with pyrene ligands to enable them to attach via π-π-stacking to the graphene [3]. This complex shows strong absorption at 477 nm which is due to the Metal-to-ligand charge-transfer (MLCT) which enables the complex to transduce an optical to an electrical signal in the graphene [4].

Preliminary measurements at room temperature showed a promising photoresponse in such structures. In this work the photoresponse was investigated in a more thorough way by optimizing the geometry of the devices (figure 1), by the use of different wavelength and temperature dependent measurements.

Different techniques to functionalize the graphene sheet are used, including standard molecule drop-casting of different concentrations and micro contact printing (μCP) of the molecules. The first results of these techniques are shown in figure 2. It can be seen that the drop-casting approach does not yield a homogeneous deposition of the molecules. For that reason μCP is used which could lead to a thin and homogeneous layer of the Ruthenium complex.

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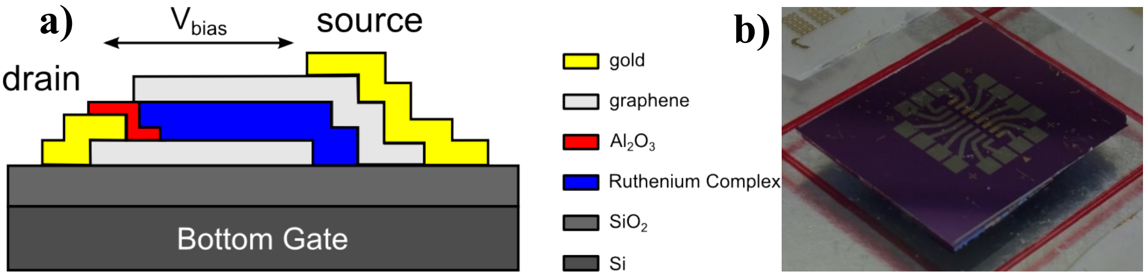

Figure 1: (a) Sketch of cross-section of the device. (b) Photo of the reference devices without molecules.

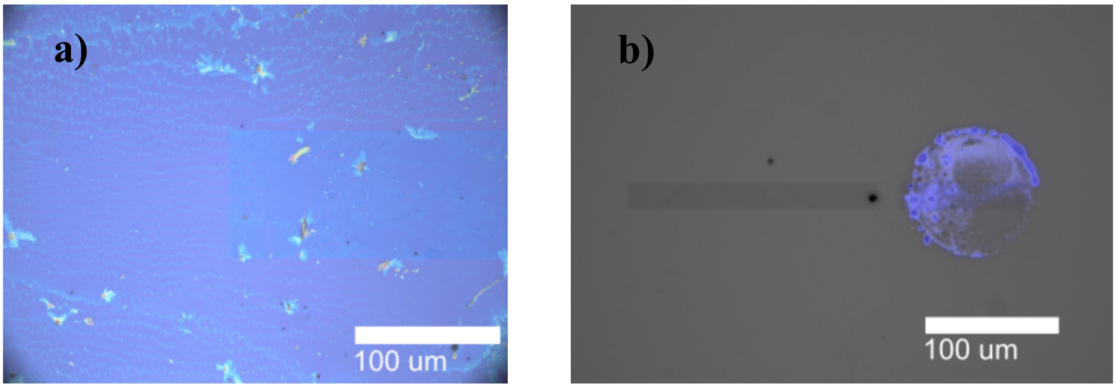

Figure 2: (a) Ruthenium complex molecules dropcasted on prepatterned CVD graphene on silicon substrate which shows a poor uniformity. (b) First attempt of micro contact printing of the Ruthenium complex on the prepatterned CVD graphene sheet (fluorescence microscopy image).

Fiber Bragg Grating Sensors: a Reliable Method for Structural Monitoring

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Fiber Bragg Gratings (FBGs), shown in fig. 1, have been widely investigated since Hill and Meltz in 1997 developed the FBG fabrication techniques and have been proposed for several applications, spanning from chemical to physical ones [1]. In particular, FBGs are widely used in structural monitoring due to their many advantages and capability that could not be achieved otherwise like small, robust, lightweight, and potentially low-cost solution and their ability to be easily attached to a wide variety of substrates makes them available for many applications. Here we present two innovative applications of the FBGs: one to the early age monitoring of geopolymers and the other one to the deflection monitoring of planar structures.

In the first one , starting from preliminary study [2], we have simultaneously measured the early-age shrinkage and temperature changes of metakaolin-based geopolymers (fig. 2). Geopolymer matrices, indeed, represent one of the main sustainable alternatives to traditional cementitious binders such as ordinary Portland cement (OPC) and other clinker-based materials offering several potential advantages like higher fire resistance, durability, etc. The early-age monitoring of geopolymers represents a key parameter for mix design optimization. This work, made in collaboration with the INSTM Research Group Naples Parthenope, has allowed the optimization of the geopolymer matrix in terms of quartz filler content in order to minimize shrinkage and, at the same time, respect the criterion of resource efficiency. (fig. 3).

In the second one, we have proposed to calculate the deflection of planar structures from the longitudinal surface strain measurements by means of FBGs arrays properly bonded to or embedded in planar structures. To this aim a simple post processing analysis of FBG strain measurements has been proposed [3]. A relationship between the longitudinal strain and the vertical deflection is derived by classical beam theory. Indeed, a second derivative relationship exists between the displacement orthogonal to the surface and the strain component parallel to it. In order to validate the proposed methodology, in collaboration with the Section in Naples of INFN, measurements of the surface strain and then of the deflection of a relatively miniaturized novel detector panel, that will be installed as a tracking detector in the ATLAS experiment at LHC (Large Hadron Collider) at CERN (European Organization for Nuclear Research) by the end of 2018, have been successfully carried out (fig. 4).

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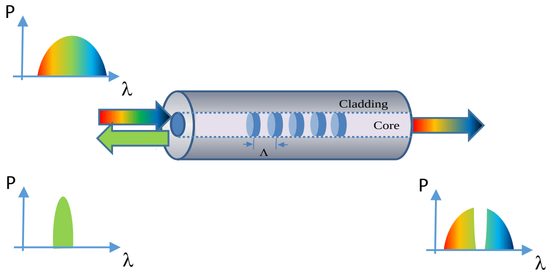

Figure 1: Schematic of FBG structure with spectral profiles.

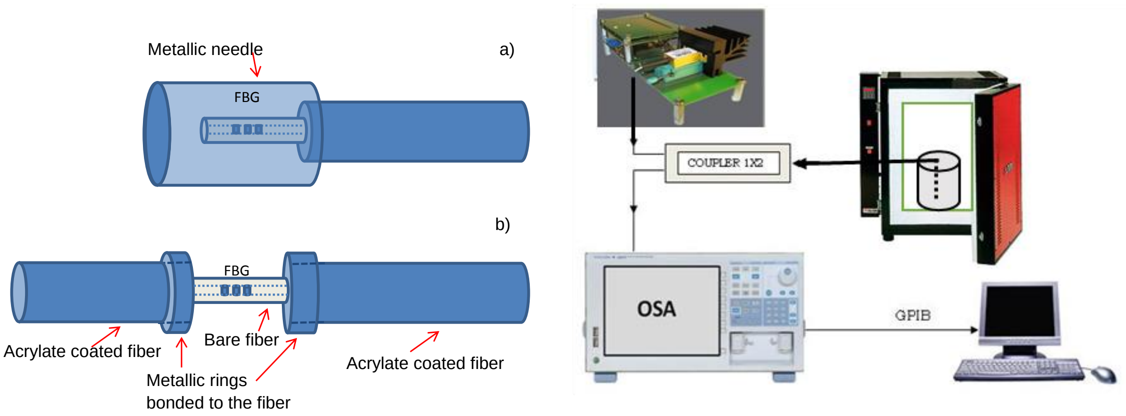

Figure 2: Left: schematic of the sample temperature FBG sensor (a) and of the sample shrinkage FBG sensor (b). Right: schematic of the optoelectronics set-up.

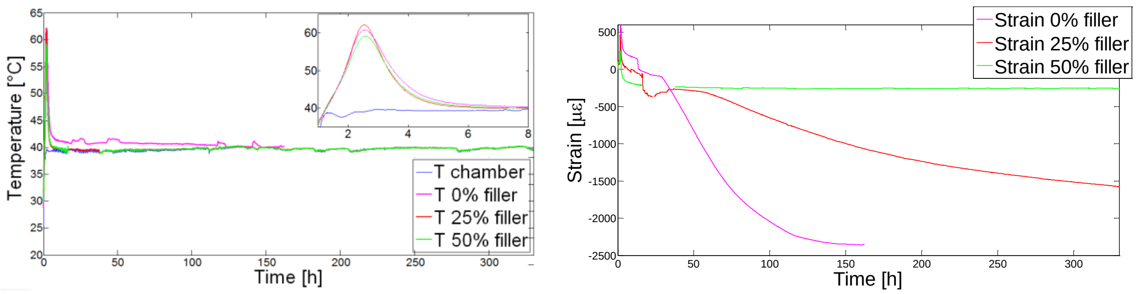

Figure 3: Temperature (left) and shrinkage (right) curves for different filler percentages obtained by means of FBG

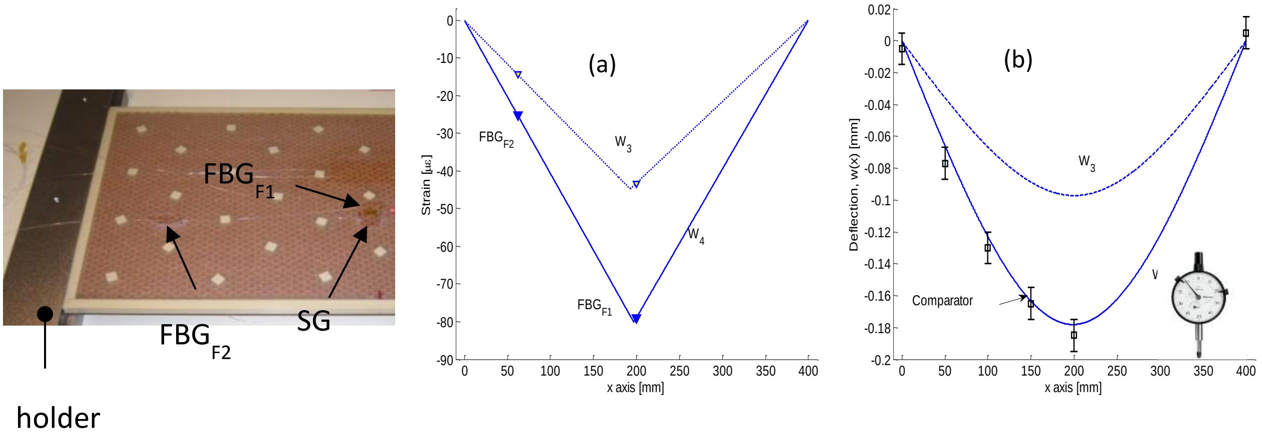

Figure 4: Left: picture of the panel with FBGs and Strain Gauge sensors. Right: (a) Strain profile of the panel as function of weight; and (b) deflection calculated from data of (a).

Germanium on Silicon bipolar phototransistor integrated on SOI platform

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Silicon photonics has recently reached a high level of readiness as a key technology in the telecommunication field, thanks to significant advances in the fabrication of both passive and active optical components on silicon platform [1]. Germanium has also been exploited as a monolithically integrable, sensitive material for NIR detection, usually in the form of a Ge-on-Si photodiode followed by a trans-impedance amplifier [2]. Nevertheless, the power budget and real estate of such devices are not suitable for high density photonic circuits.

In this work we propose a bipolar Ge-on-Si phototransistor as a compact receiver for silicon photonics. The transistor has been realized by IME A*STAR through CMC Microsystems in a multi-project wafer run dedicated to silicon photonics. The design kit provided by the foundry did not include a transistor so we had to adapt our design in order to satisfy the IME A*STAR rules. The device (shown in fig. 1) is fabricated on a 220nm thick p-type ($10\Omega cm^{-1}$) SOI substrate. A 500nm thick unintentionally doped Ge serves as the NIR sensitive material. A high dose phosphorus implantation in the top 100nm of the Ge film ensures linearity of the top contact. The device has been designed in a wave guided geometry in order to maximize the optical absorption efficiency. Light is coupled through an integrated grating coupler.

Dark, DC, characterization demonstrated the expected transistor operation. Figure 2 shows the device current characteristics under illumination with electrically floating Ge contact. The Ge top contact was initially intended as a mean to select the best operating point for the enhancement of the transistor optical response, nevertheless the best results were obtained leaving Ge floating. Responsivities as high as 100A/W where obtained for $V_{CE} = 5V$ considering a -6dB insertion loss at the grating coupler. Device responsivity proved to be strongly dependent on the incident optical power due to high injection in the transistor base; in fact, the germanium doping is low enough to let the photogenerated carriers overwhelm the ones generated by acceptors and trap states even for low optical power. Therefore the transistor shows better performances at low incident power proving to be a promising device for low-power, short distance communications. However, the dark current (~50µA @ 5V) is still too high for proper device operation at the highest responsivity.

In conclusion, the proposed device showed very good results if compared to standard p-i-n Ge-on-Si photodetectors even without any design optimization, thus leaving room for future enhancement. The proposed transistor is extremely promising for the development of both integrated optical receivers and high sensitivity integrated optical sensors.

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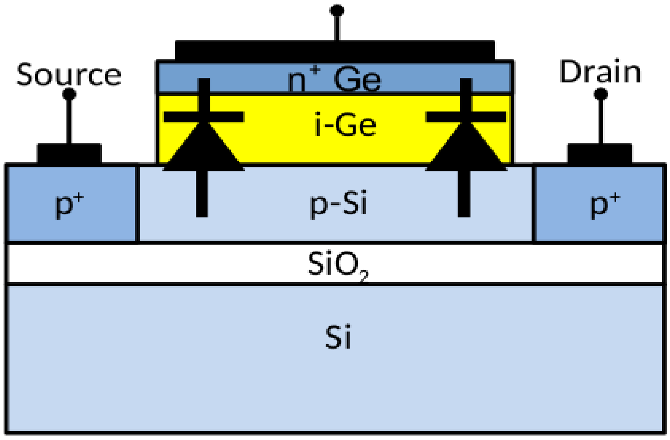

Figure 1: Device schematic cross section.

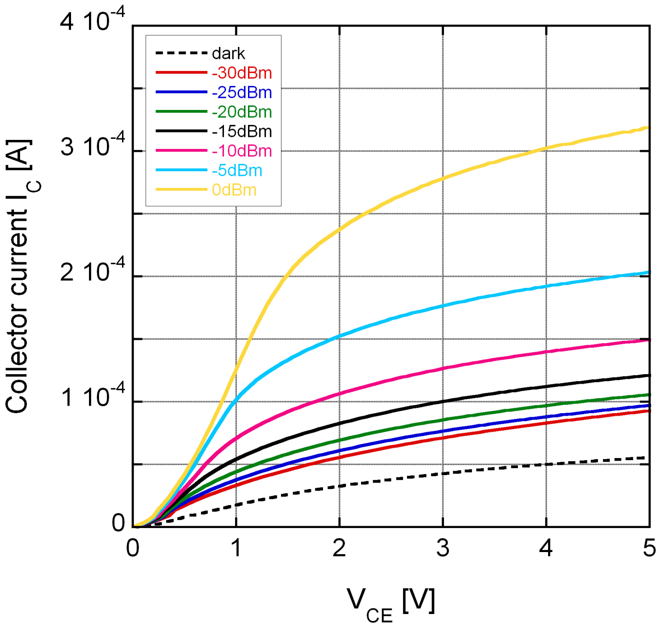

Figure 2: Ic-Vce characteristics under illumination

Innovative Optical Fiber Nanoprobes for Biological Sensing

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In this work, we demonstrate the effectiveness of c [1] based devices for biosensing applications, and in particular for detecting tumor markers for thyroid cancer i.e. thyroglobulin (TG). The “Lab on Fiber Technology” has been recently proposed as a valuable route for the realization of novel and highly functionalized technological platforms completely integrated in a single optical fiber [2]. The principle of operation of the optical fiber biosensor transducer is based on the intensity variation of the back-reflected light, due to a refractive index change at the sensor surface when a target biomolecules layer binds onto the sensor surface. Here we present two different Lab-on-Fiber devices able to detect the biomolecules binding onto our sensitive surfaces. In particular, the first one is based on the integration, directly on the optical fiber tip, of a square lattice of gold pillars (see Fig.1a) supporting local surface plasmon resonances. Thanks to the highly localized character of its field distribution at the resonant wavelength, this configuration can easily detect local environment changes (nano-sized overlays deposited on the sensor surface). The second configuration is based on the integration, onto the surface of reflection-type Long Period Fiber Gratings (LPFGs), of nano-scale polymer overlay (see Fig.2.a) that enables the modal transition phenomenon [3] to take place. In particular, by acting on the High Refractive Index (HRI) layer thickness (ranging in hundreds of nanometers), it is possible to exploit the HRI-coated LPGs for chemical and biomolecular sensing applications. Two different strategies were chosen for sensor surface functionalization; in the first technological platform, a mixed self-assembled monolayer of alkanethiols-based functionalization of the sensitive interface allows the covalent immobilization of the specific bioreceptors (i.e. anti-TG monoclonal antibodies, previously selected as high affinity and specific TG receptors and deeply characterized by immunoenzymatic and label-free assays) with minimal perturbation of the optic design. In the second case, the nano-scale atactic polystyrene (aPS) polymer overlay which coated the reflection-type LPG has been functionalized with a hydrophobic coating of the the above mentioned bioreceptors.. The experimental results so far carried out (summarized in the figure below, details in the figure caption) provide a clear demonstration of the effectiveness of both the developed biosensing platforms, allowing the in-vitro detection of human Thyroglobulin (see Fig. 1.b and 2.b) at sub-nanomolar concentrations.

This work is part of the national project “Smart Health 2.0” funded by the Italian Ministry of Education, University and Research (MIUR) under the PON framework.

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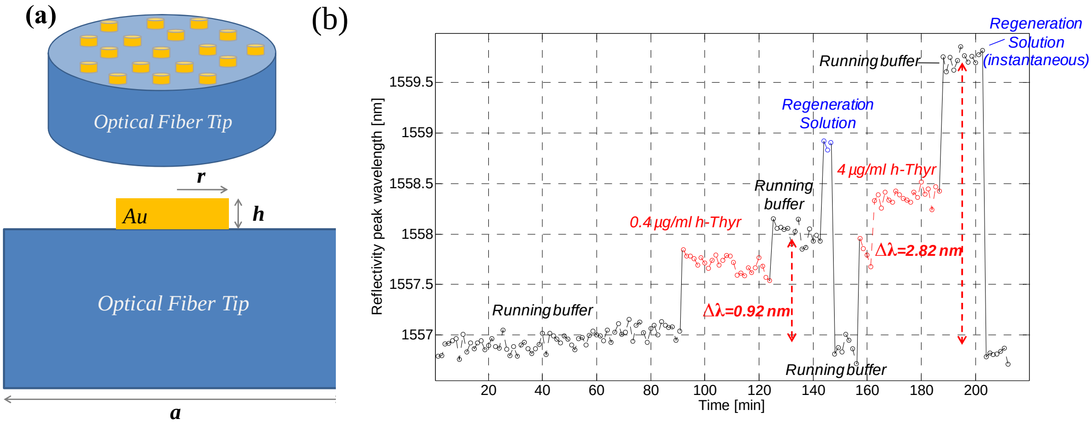

Figure 1: a) Schematic view of the Lab-on-Fiber platform based on the integration of a square lattice of gold pillars on the fiber tip. b) Typical dynamic resonance wavelength shift of the device due to the detection of human thyroglobulin. Also the baseline regeneration step is shown.

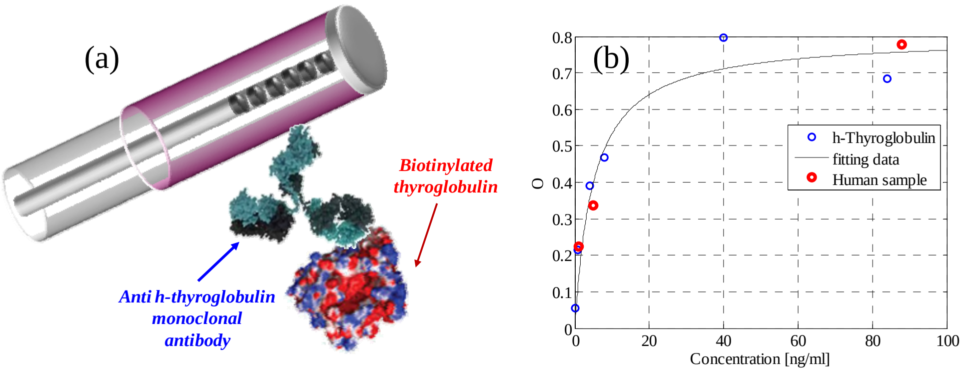

Figure 2: a) Schematic view of the reflection-type LPG biosensor. b) Calibration curve for the semi-quantitative detection of human thyroglobulin (blue dots) using LPG biosensor. Also ex-vivo detection of human thyroglobulin from the needle washout of fine-needle aspiration biopsy is shown (red dots)

Long Period Grating in Photonics bandgap fiber: from the idea to the perspectives

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This paper reports on the fabrication of Long Period Gratings (LPGs) in hollow-core silica photonic bandgap fibers (HC-PCFs). LPGs are devices that consist of a periodic change in the refractive index and/or in the fiber geometry along the fiber length with the typical period of several hundred micrometers [1]. The periodic perturbation along the fiber induces light coupling from the fundamental mode to higher order modes at specific wavelength. These devices can have sensitivities custom designed to the specific parameters of interest and thus are subject of great interest for the scientific community. LPGs are commonly manufactured in standard fibers and solid-core photonic crystal fibers, by means of several approaches such as UV photosensitivity, EAD, CO_2 or femtosecond lasers.

The fabrication of LPG in hollow core photonic bandgap fibers is a challenge for the scientific community. Recently we proposed the fabrication of LPG in HC fiber by using pressure assisted Electrode Arc Discharge (EAD) technique [2]. It combines the use of EAD step, to locally heat the HC-PCF fiber, and of a static pressure slightly higher (P=126kPa) than the external one inside the fiber holes, to modify the holes. This procedure permits to induce a periodic modification of the effective refractive indices of fiber modes via size and shape modifications of core and cladding holes. Fig. 1 plots the scheme of the setup used for the fabrication of the gratings. It involves a commercial splicer machine to apply EAD with properly selected arc duration and time values. A manual pressure pump and pressuremeter are used to fix the air pressure inside fiber holes to 126kPa. Besides, a microstepper permits to repeat the perturbation step (pressure assisted EAD procedure) with a fixed period along the fiber. The effect of the pressure assisted EAD step is documented in fig. 2 by comparing optical microscopy images of pristine and perturbed HC cross-section [3]. The main effect is the core size enlargement from the $D_{CO}=11 \pm 0.5$ µm to $D_{CO}=13 \pm 0.5$ µm. Conversely, the external diameter and micro-structured cladding diameter decrease from $D_{ex}=120\pm0.5$µm to $D_{ex}=117\pm0.5$ µm and $D_{CL}=70.0\pm0.5$ µm to $D_{CL}=65.0\pm0.5$ µm, respectively. Fig. 3(a) compares the spectrum of pristine HC fiber (spliced in between two SMFs) and the spectra of two LPGs with pitch of $\Lambda=400$ µm and different length of 20 and 25 periods, $L = 20\ \Lambda$ and $25\ \Lambda$, respectively. Fig. 3(b) plots the spectra of LPGs with 25 periods, and period ranging in $\Lambda= 350$, 400 and 450 µm. The sensitivity properties to temperature, strain, curvature and pressure are experimentally evaluated showing that it is possible to beneficiate form the combination of the hollow core fibers and grating based sensors [4].

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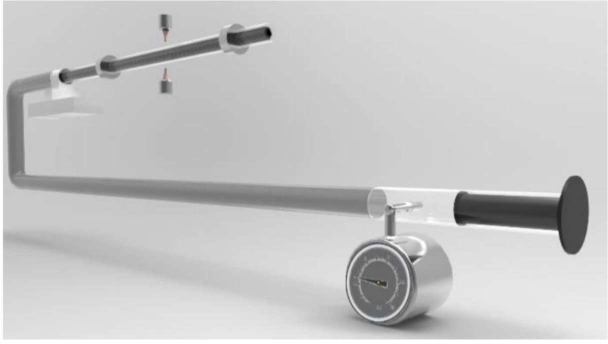

Figure 1: Schematic diagram of LPG fabrication experimental setup.

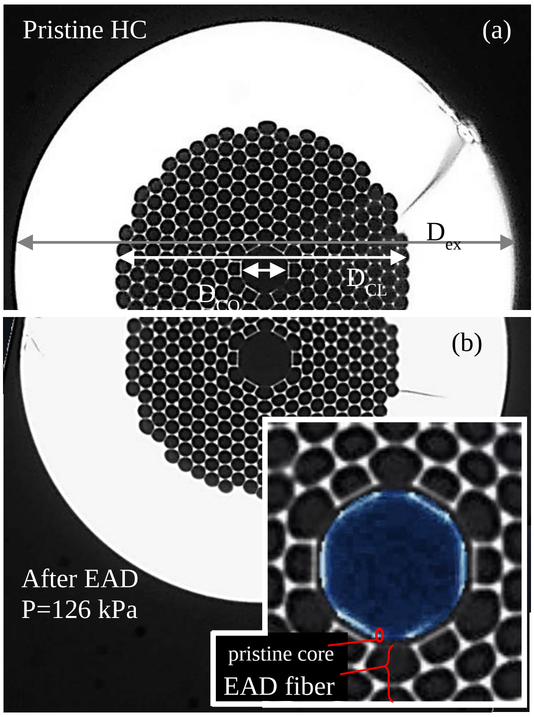

Figure 2: Optical microscopy images of HC cross-section (a) before and (b) after EAD procedure; insert comparison of fiber core before and after EAD procedure

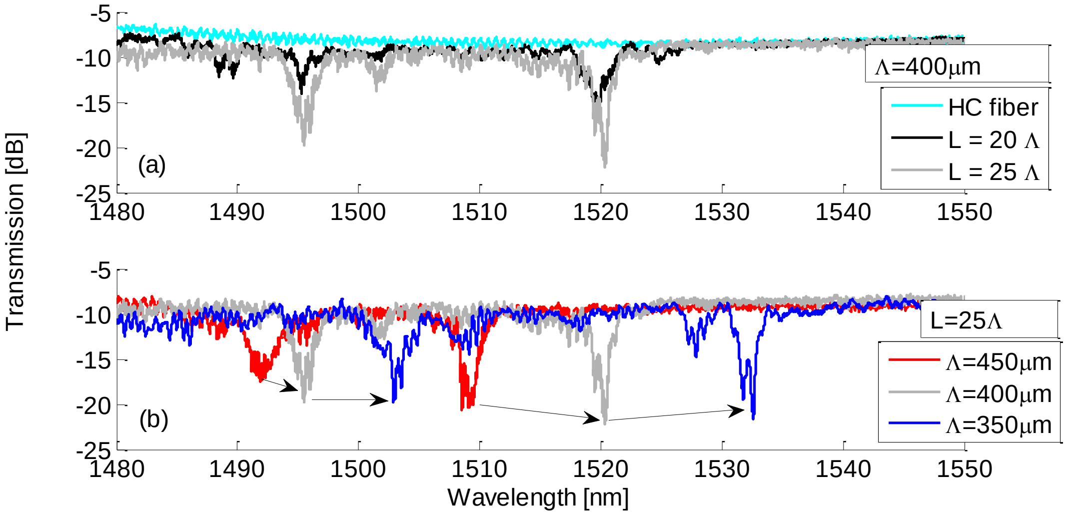

Figure 3: Transmitted spectra of LPG in HC. (a) LPGs with Λ=400µm and different length, L=20 and 25 Λ; and (b) LPGs with L=25 Λ and different period, Λ=350, 400 and 450µm

Measurements of cardiac Pre-Ejection period using a combo PPG-ECG system

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The extraction of biomedical parameters, for early disease detection, is assuming today an ever increasing and fundamental importance. In particular, in the cardiologic field, the pre-ejection period (PEP) is the duration of the iso-volumetric left ventricle contraction until the aortic valve opening. This parameter is a non-constant additive delay, which rapidly changes in response to stress, emotion and physical effort [1]. To estimate this period, several wearable electronics devices have been developed in literature, and among them the Impedance Cardiogram equipment is the most used [2]. However, these systems are often expensive and bulky. In this paper, we propose a cost-effective and easy to employ ECG+PPG combo system able to measure pre-ejection period in a cardiac cycle.

The employed system is composed of an ECG acquisition board (Fig. 1) able to host two PPG probes too. The board is based on the analog front-end ADS1198 from Texas Instruments, tailored for scalable medical instrumentation systems. It has 8 simultaneous sampling channels, 16-bit, delta-sigma analog-to-digital converters. Each PPG probe includes a 940 nm LED and a Silicon Photomultiplier (SiPM) detector. The SiPM allows a very good responsivity and high gain [3]. The measurements have been carried out by simultaneously acquiring the ECG signals from standard limb leads, and the PPG signals from the wrist and the forearm. Starting from the PPG waveforms and the ECG lead II, we are able to measure the Pulse Transit Time (PTT_{fw}) as the time interval required for the pulse wave to propagate from the forearm to the wrist. In detail, the PTT is obtained by measuring the delay between two characteristic points of the signals (i.e., the minimum points). Since the distance between the heart and the forearm is fixed and known and supposing, in first approximation, the wave velocity constant, it has been possible to experimentally determine the pulse transit time from the heart to the forearm (PTT_{hf}). This assumption has been made since we have kept the arm at the same height of the heart. Afterwards, the Pulse Arrival Time (PAT_{hf}), i.e., the time delay between the onset of the ECG Q-wave and the minimum of the forearm PPG signal, has been measured for each cardiac cycle. Finally, the PEP has been determined as the difference between the PAT_{hf} and the PTT_{hf} [1]. Several measurements have been carried out on a number of volunteers in order to measure the above-mentioned parameters (i.e., PAT, PTT and PEP). As an example, Fig. 2 shows the typical ECG and PPG signals taken during an acquisition. Results show that the PTT_{fw} is on average 38 ms, obtaining a PTT_{hf} of about 65 ms corresponding to a pulse wave velocity of about 8.5 m/s, in agreement with the values reported in literature [4]. The PAT_{hf} is around 190 ms, thus obtaining a PEP of about 130 ms.

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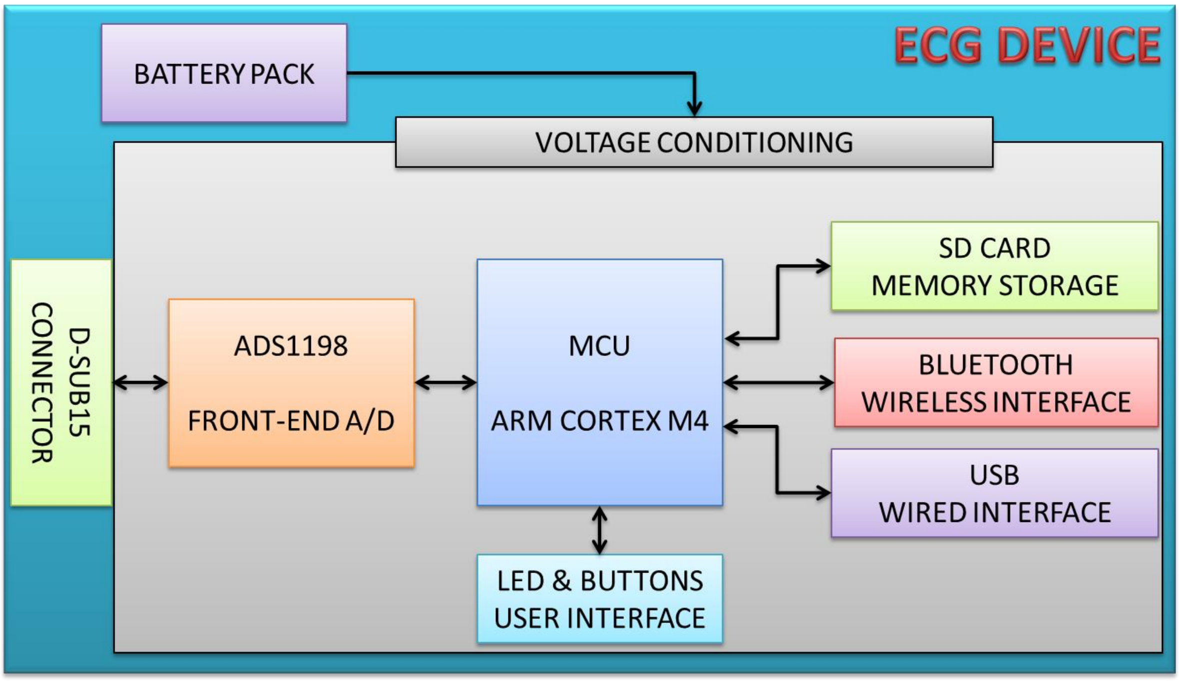

Figure 1: Schematic block diagram of the ECG system.

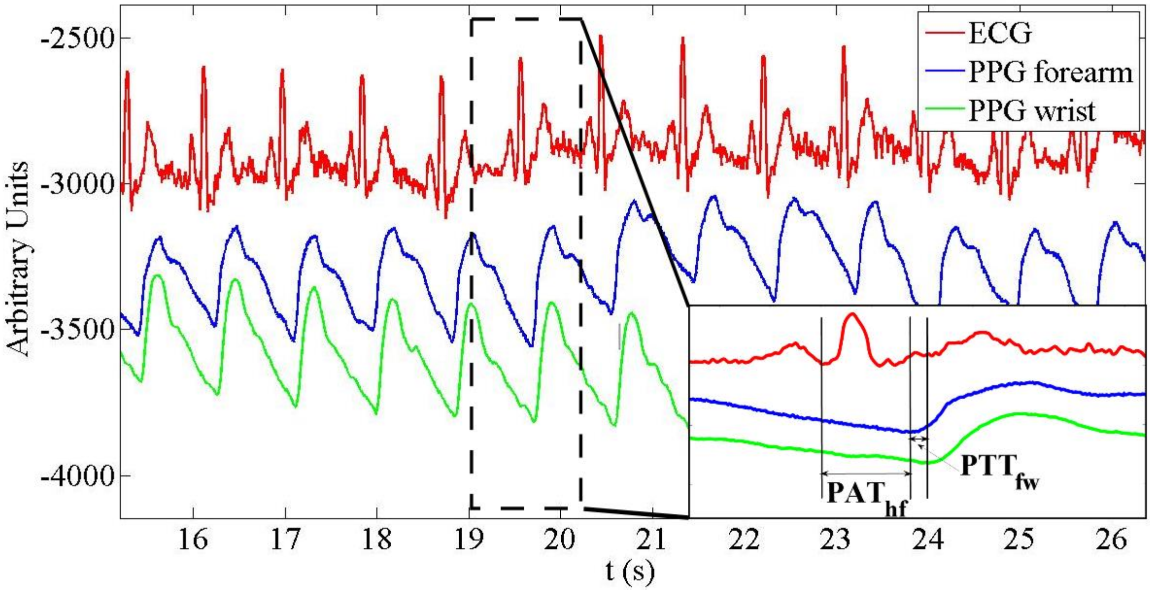

Figure 2: ECG signal and PPG signals (forearm and wrist) vs time.

Microgel Photonics: towards multiresponsive optical fiber nanoprobes

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Microgels (MGs) have recently received attention as environmentally responsive systems and now are increasingly used as direct sensing materials. MGs are colloidally stable hydrogel particles that can be made to respond to subtle changes in their environment due to temperature, pH, and ionic strength. [1] Recently, poly (N-isopropylacrylamide)-co-acrylic acid (pNIPAm-co-AAc) MG based etalon have been proposed [2-4].

Following the works by Sorrell et al. [3-4] here we propose a first prototype of Lab-on-Fiber device based on MG photonics technology. The device is realized by integrating a MG film between two gold layers on the facet of a standard mono mode fiber (see Fig. 1a). The bottom gold layer, deposited trough electron beam evaporation (2nm Cr / 15nm Au) is patterned by using a Focused Ion Beam (FIB) milling (FEI Quanta 200 3D) in order to obtain a square lattice of holes with period a=750 nm and radius r=150 nm. (pNIPAm- co -AAc) MGs crosslinked with 5% N, N ’-methylenebisacrylamide (BIS) and containing 5% AAc were synthesized (radius 0.5 µm in solution as determined by dynamic light scattering) and the concentrated MG solution was painted on the patterned layer. Successively, the MG layer was dried, and an additional gold layer (2 nm Cr/ 15 nm Au) was deposited on the MG film. The SEM images (top view) of the fabricated devices are shown in Fig. 1b.

The fabricated device shows spectral features in the NIR wavelength range (1200-1750 nm) that are associated to the excitation of Fabry-Perot modes hybridized with the plasmonic localization supported by the metallic grating. The fabricated probe, dipped in water at ambient temperature shows a reflectance spectrum reported in Fig. 2a. When immersed in water, by decreasing/increasing the temperature, the MG layer swells/squeezes and its thickness changes, causing a variation in the distance between the two metallic structures separated by the MG layer, and thus a shift of the resonant wavelengths. In order to preliminarily investigate the temperature responsivity, the optical fiber nanoprobe has been characterized through a temperature controlled setup. Fig. 2b shows the reflectance spectra of the sample dipped in water during the temperature increasing process (from 6 to 50 °C). When the MGs are swollen at low temperature, the reflectance exhibit a maximum at ~ 1700 nm. As the temperature increases, MGs undergo temperature-initiated Phase Separation events (Volume Phase Transition) with a consequent diameter decreasing that causes a maximum blue shift of the reflected spectrum of ~30nm/°C.

Overall, by changing the pattern characteristics and/or by using MGs with different hydrodynamic diameter it is possible to vary the cavity length, and thus engineer the device spectral response. Finally, the integration of MGs on the optical fiber tip represent a step forward for developing novel Lab-on-fiber technological platforms based on MG photonics for acoustic and bio- sensing applications.

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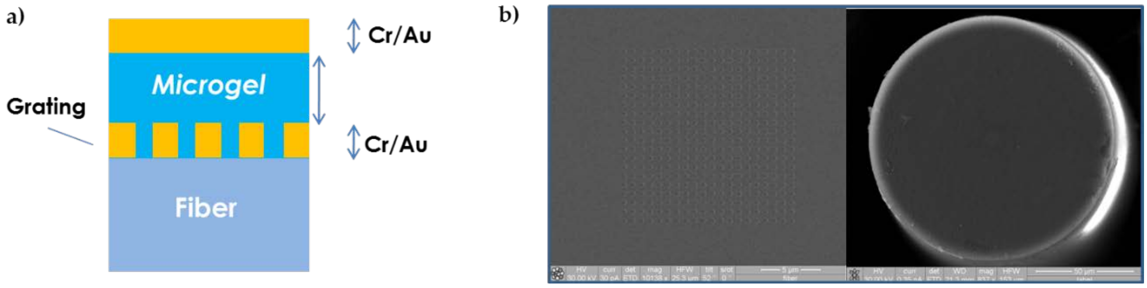

Figure 1: a) Schematic of Lab-on-Fiber device based on microgel photonics technology Schematic of the microgel; **b)** SEM images (top view) of the fabricated devices after microgel deposition

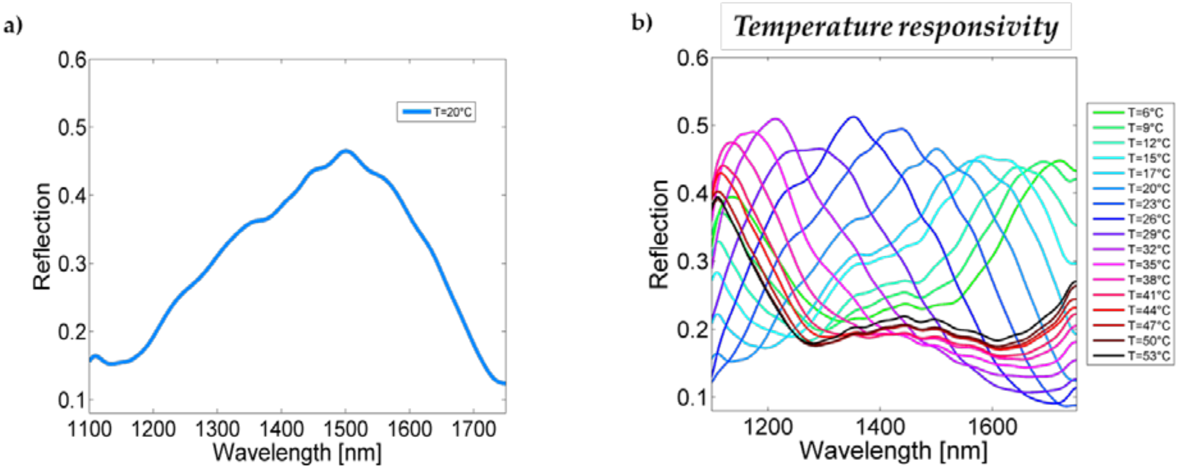

Figure 2 a) Measured reflection spectra in water (pH 3) at temperature of 20°C; **b)** Reflectance spectra of the sample dipped in water during the temperature increasing process (from 6 to 50 °C).

Optoelectronic beamformer for spaceborne X-band synthetic aperture radar

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Spaceborne Synthetic Aperture Radar (SAR) for Earth Observation exploits a Phased Array Antenna (PAA) with thousands of radiating elements in which the key functions of beam shaping and steering are provided by a beamformer.

Conventional RF beamformers, relying on phase shifters, exhibit a poor bandwidth, mostly due to the fact that they implement a phase shift rather than a true time delay. Since early 90s, several configurations of the optical beamformer have been proposed in literature based on discrete, fiber, or integrated optics [1], in the perspective to achieve high bandwidth operation. Optical approaches allow volume and mass reduction, immunity to electromagnetic interference, and low transmission loss.

The typical configuration of an optoelectronic beamformer is shown in Fig. 1. The RF signal modulates the optical carrier, which is then split in a number of signals. The split signals are delayed so that constructive interference occurs where it is required. The bandwidth of the signal to be processed is approximately twice the RF central frequency. This imposes stringent requirements that can be alleviated implementing the single sideband modulation or the separate carrier tuning technique [2].

The spaceborne SAR in the X band (7.5 GHz – 12 GHz) has typical values of the steering angle in the range of 15°–20°, for the elevation plane, and in the range of 1°–2° for the azimuth plane. We have considered the case of a linear array, in the nadir direction, comprising eight radiating elements, spaced at a distance of 0.8 λ, and operating at 9.65 GHz.

The designed beamformer network, shown in Fig. 2, is based on a binary tree topology, in which the same delay path branch out progressively [3]. This choice, together with the selection of a delay element based on coupled resonators, allows to reduce the complexity of the structure, providing efficiency and flexibility. Silicon on Insulator (SOI) technology has been chosen in order to increase compactness and to allow integration of multiple functionalities.

In the three sections, it is necessary to introduce a differential delay in the ranges 0 ÷ 120 ps, 0 ÷ 60 ps, and 0 ÷ 30 ps, respectively. In order to achieve the higher delay, two ring resonators, whose frequency response is properly shifted, are used. Continuous tunability is also a crucial aspect in the design. In order to obtain the desired variation of the delay in the appropriate range, it is necessary to implement a variation of the power coupling coefficient between the bus and the resonators of the order of about 20%. We are investigating the best tuning technique in terms of compactness and response time.

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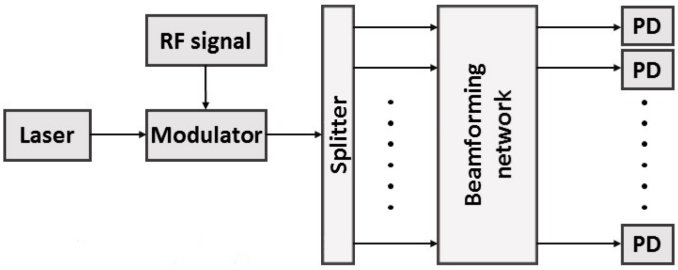

Fig.1 Schematic configuration of an optical beamformer comprising a laser source; a splitter a beamforming network, and an array of photodetector.

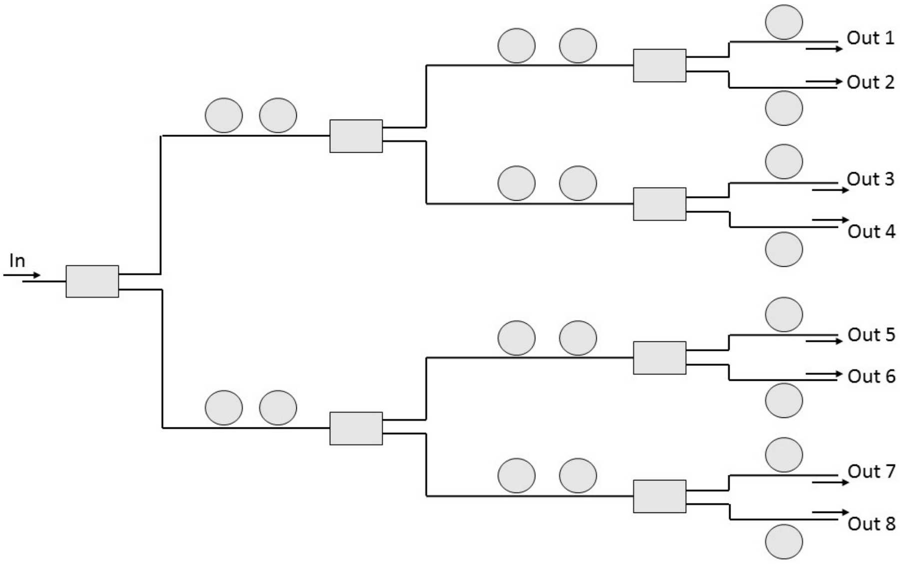

Fig.1 Beamformer network based on a binary tree topology and comprising three sections with 2,4 and 8 branches in which ring resonators act as delay line.

Photonic Sensing Systems for Smart Railways

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The ever increasing demand for improved safety, security and efficiency is among the most important aspects of the railway industry worldwide. The needs of a smart condition monitoring systems are imminent as indicated by the increase in railway accidents/incidences. Similarly the monitoring and the protection from undesired accesses of railway assets, such as tunnels, level crossings and train depots, would lead to significant cost savings by reducing theft and vandalization and, at the same time, by improving the safety and security.

The Optoelectronics Research Group at the University of Sannio is successfully working in tight collaboration with Ansaldo STS company to the design and development of advanced photonic sensing systems with unrivalled performances for smart railways. Recently a smart sensing system for weighing in motion (WIM) and wheel flat detection (WILD) was installed along the rail of Garibaldi Central Station (Ente Autonomo Volturno - EAV) in order to provide a continuous and real time monitoring of the trains transit. An intrusion detection system was installed at the EAV Ponticelli Service Area in Naples (Italy) to protect the area from the undesired access. Both systems, being based on a single enabling technology, the optical fiber, are sharing the same advantages such as immunity to electromagnetic interference, remote sensing, stability in harsh environments, multiplexing capability, high sensitivity, wide dynamic range and installation [1].

Fig. 1a shows the WIM-WILD system's architecture and the typical installation layout. The system is able to return, in real time, information about ETRs running along EAV lines such as: speed, acceleration, direction of transit, number of axles, weight distribution per wheel, axle and wagon, monitoring of any longitudinal and transverse imbalances, detection of defected wheels and identification of the kind of defect. The Measure Zone is composed by 10 Fiber Bragg Gratings (FBG) sensors (5 for each rail track), which detect the vertical forces generated by the wheel/rail contact. Each sensor is placed in a robust metal housing mounted under the rail and designed to guarantee: reduced overall dimensions, minimal impact on the track, no rail drilling, ease of installation and removal, capability to operate in harsh environment. The results of experimental trials and functional verification tests (Fig. 2) demonstrated the correct operation of the system for two main functions of weighing and detection of defected wheels during the ETR's transits.

Fig.1b shows the Intrusion Detection System installed at the entry point of the Ponticelli depot. The sensing system is conceived to operate alone to protect a “walkable” entry point or in joint with a thermal/video camera to improve the recognition capability of existing video analysis systems. The photonic sensing system is composed of a mat, as large as 18 m^2, sensorized with 75 FBG strain sensors. An intruder, walking on the mat, represents a load on the upper surface of the soft rubber mat, endowed by a low young modulus [2]. The FBGs sense the strain associated to the load and convert the strain in a Bragg wavelength shift. Several trials on field was carried out to verify the functionality of the system in presence of intruders walking on the mat. Experimental results reveal that FBGs sensors, bonded under a ribbed rubber mat, enable the detection of intruder's break-in (fig. 2).

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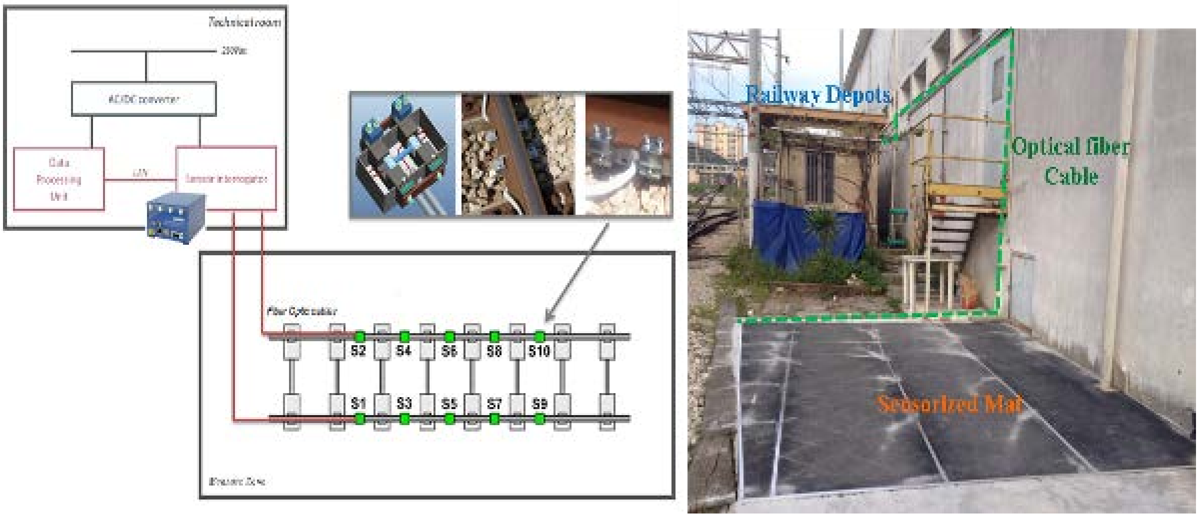

Figure 1:a) WIM - WILD system and installation layout, b) Intrusion Detection System

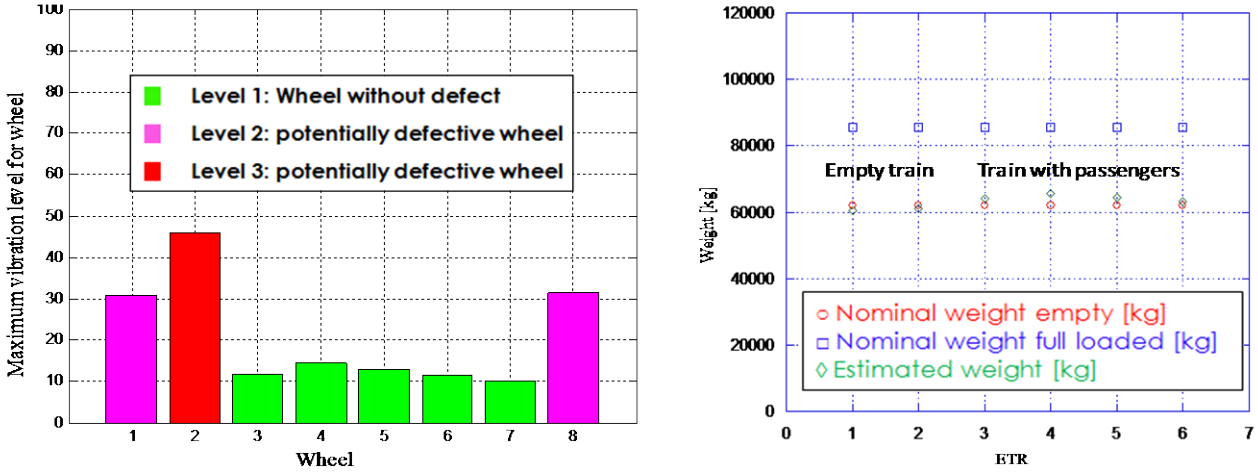

Figure 2: a) detection's test of defected wheels b) weight tests

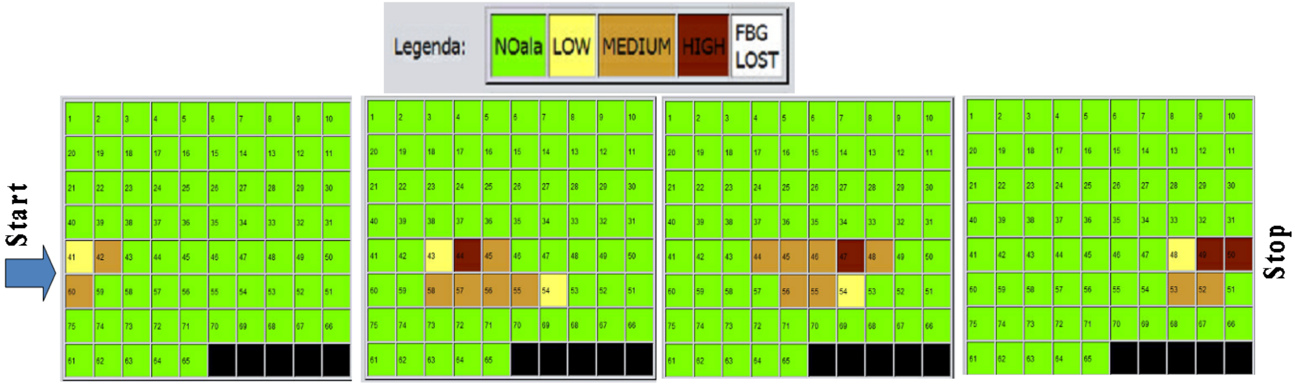

Figure 3: Intrusion Detection System software Interface: automatic detection and localization of an intrusion event

Optoelectronic beamformer for spaceborne X-band synthetic aperture radar

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Spaceborne Synthetic Aperture Radar (SAR) for Earth Observation exploits a Phased Array Antenna (PAA) with thousands of radiating elements in which the key functions of beam shaping and steering are provided by a beamformer.

Conventional RF beamformers, relying on phase shifters, exhibit a poor bandwidth, mostly due to the fact that they implement a phase shift rather than a true time delay. Since early 90s, several configurations of the optical beamformer have been proposed in literature based on discrete, fiber, or integrated optics [1], in the perspective to achieve high bandwidth operation. Optical approaches allow volume and mass reduction, immunity to electromagnetic interference, and low transmission loss.

The typical configuration of an optoelectronic beamformer is shown in Fig. 1. The RF signal modulates the optical carrier, which is then split in a number of signals. The split signals are delayed so that constructive interference occurs where it is required. The bandwidth of the signal to be processed is approximately twice the RF central frequency. This imposes stringent requirements that can be alleviated implementing the single sideband modulation or the separate carrier tuning technique [2].

The spaceborne SAR in the X band (7.5 GHz – 12 GHz) has typical values of the steering angle in the range of 15°–20°, for the elevation plane, and in the range of 1°–2° for the azimuth plane. We have considered the case of a linear array, in the nadir direction, comprising eight radiating elements, spaced at a distance of 0.8 λ, and operating at 9.65 GHz.

The designed beamformer network, shown in Fig. 2, is based on a binary tree topology, in which the same delay path branch out progressively [3]. This choice, together with the selection of a delay element based on coupled resonators, allows to reduce the complexity of the structure, providing efficiency and flexibility. Silicon on Insulator (SOI) technology has been chosen in order to increase compactness and to allow integration of multiple functionalities.

In the three sections, it is necessary to introduce a differential delay in the ranges $0 \div 120$ ps, $0 \div 60$ ps, and $0 \div 30$ ps, respectively. In order to achieve the higher delay, two ring resonators, whose frequency response is properly shifted, are used. Continuous tunability is also a crucial aspect in the design. In order to obtain the desired variation of the delay in the appropriate range, it is necessary to implement a variation of the power coupling coefficient between the bus and the resonators of the order of about 20%. We are investigating the best tuning technique in terms of compactness and response time.

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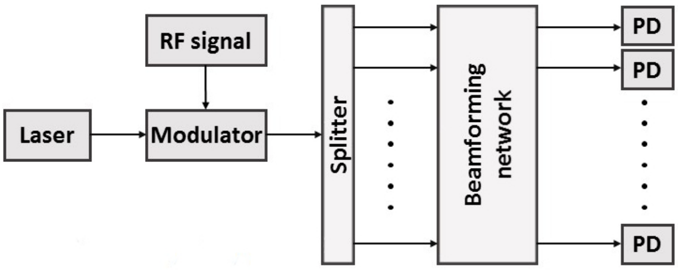

Fig.1 Schematic configuration of an optical beamformer comprising a laser source; a splitter a beamforming network, and an array of photodetector.

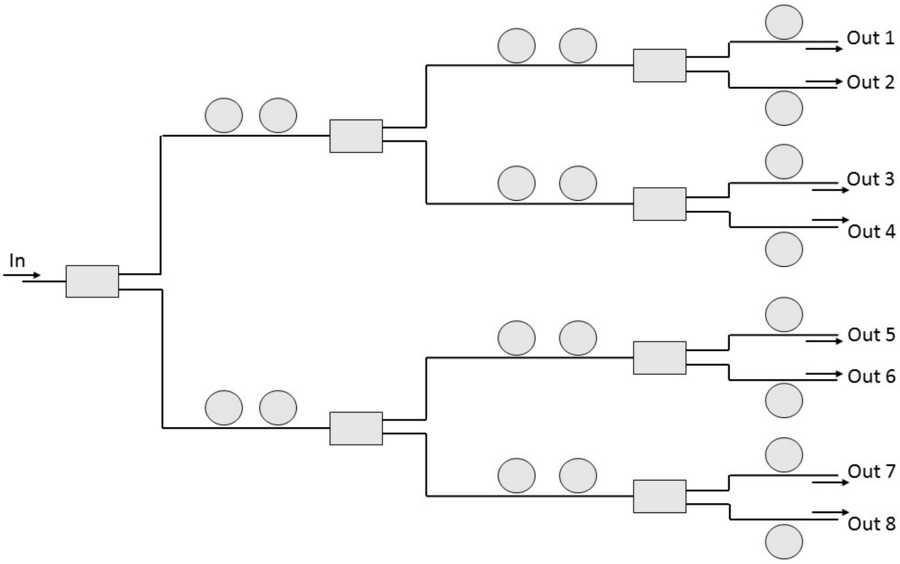

Fig.1 Beamformer network based on a binary tree topology and comprising three sections with 2,4 and 8 branches in which ring resonators act as delay line.

Polarization independent liquid crystal waveguide for photonic integrated circuits

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Liquid crystals (LC) and LC-composites can be successfully used in the fabrication of photonic devices [1-3] to be employed in several applications including sensors, optical communications, datacom and imaging systems. The integration on the same chip of microfluidic channels and optical components allows to obtain an optofluidic system with superior functionalities such as reconfigurability, higher sensitivity and better performance [4]. Components in guided-wave microstructures operating at low optical and electrical powers can be engineered and produced exploiting their excellent thermo-optic, electro-optic and nonlinear optical responses [5].

Our latest work was focused on light propagation in PDMS (polydimethylsiloxane) channels with nematic LC core. Both simulation and experimental results confirmed the presence in such waveguides of a polarization independent light transmission.

In this work we present both experimental results and the theoretical findings obtained through Monte Carlo simulations of molecular reorientation and of microscope light transmission through polydimethylsiloxane (PDMS) channels with nematic LC infiltrated core.

The results of Monte Carlo simulations are shown in fig. 1. In fig. 1.a the homeotropic alignments between liquid crystals and channel surface are represented. The red color code indicates the spin alignment along z, which is favored inside the sample since the horizontal surface is larger with respect to the vertical ones. Figure 1.b and 1.c shows the polarizing microscope images obtained starting from simulation result.

A fabrication process used to obtain PDMS channel is based on cast and molding technique [6,7]. We employed SU8 molds of the microchannels structure obtained by means of a standard photolithography process. PDMS 8 μm wide and 5 μm high micro-channels were fabricated by using SU8 molds of the negative image of the channels. The obtained PDMS layer was covered with a second PDMS layer and filled in vacuum by capillarity with the nematic LC E7 in its isotropic phase at 80 °C and subsequently cooled down to room temperature. No alignment was needed to obtain molecule orientation since LC nanometric sized molecules are spontaneously homeotropically aligned inside channels of PDMS due to its low surface energy.

In order to compare the simulation with the experimental results, fig. 2 shows an image of liquid crystal homeotropic alignment in a PDMS channels under polarizing light. The similarities between fig. 1.c and fig. 2 are evident and confirm the agreement between experimental and simulation result.

Transmission of light confined into the channel was measured by butt-coupling single mode fibers at both input and output waveguide end-faces. A laser source of 1550 nm, connected to a graduated fiber pigtailed polarization controller was employed.

The device is polarization insensitive as shown in Fig. 3, since the transmitted light power variation with polarization angle is limited to just 0.35 dB [8].

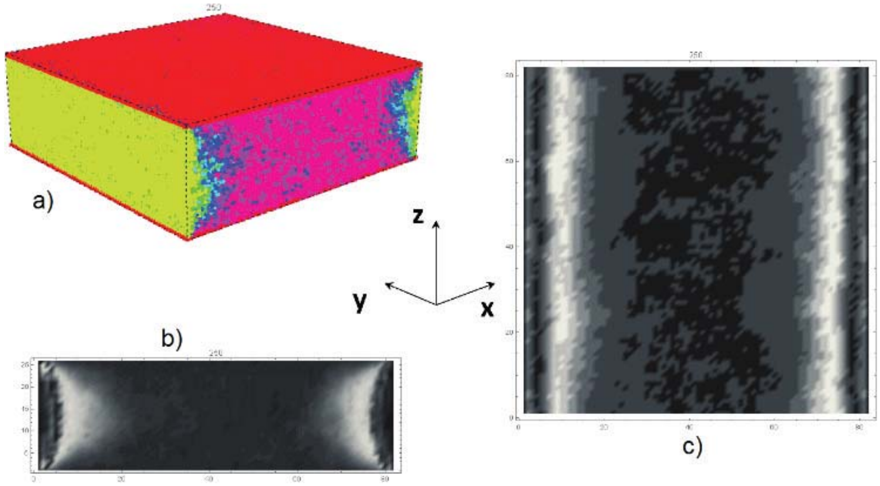

Figure 1: Overall molecular organization (a), and simulated optical images obtained on front (b) and vertical (c) point of view.

Figure 2: A polarizing microscope image of LC homeotropic alignment in PDMS channels.

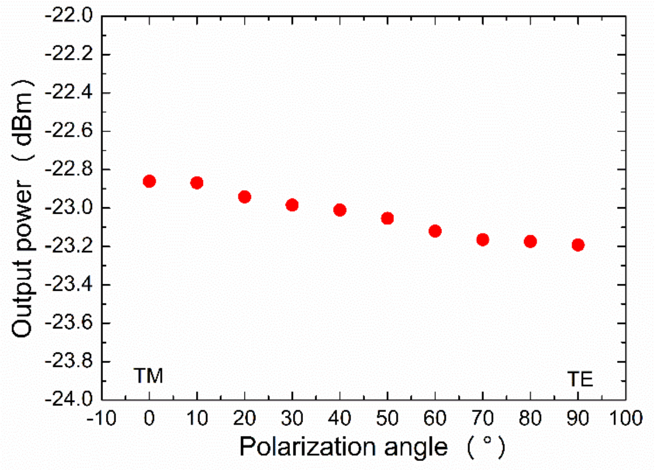

Figure 3: Transmission of light at 1550 nm versus polarization in a typical LC:PDMS 8 µm wide and 5 µm high waveguide.

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Printed Perovskite-based photodiodes

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Recently organometal halide perovskite compounds have attracted great attention as light absorbing materials in photovoltaic applications with a power conversion efficiency (PCE) reaching 20.1 % [1]. Few works on perovskite-based photodiodes (PPD) were published [2], here we present a novel perovskite-based photodiodes using one-step and two-step deposition (respectively $CH_3NH_3PbI_{(3-x)}Cl_x$ and $CH_3NH_3PbI_3$) with Spiro-OMeTAD as Hole Transport Material (HTM).

Figure 1-a shows the JV characteristics in dark and, in the inset, the performance of the same devices used as solar cell. Two step procedure shows better rectification behavior of about 10^4 between +/-1V with dark current measured at -2 V reverse bias of about $1.7*10^{-3}$ mA/cm^2. As showed in Figure 1-b, Perovskite based devices are able to extend the external quantum efficiency (EQE) from 300 nm to 800 nm that is desirable for the design of broadband photo detector in order to increase the transmission capacity. In the same figure we reported the responsivity R and detectivity D calculated with equation (1) and equation (2) for device fabricated with two step procedure.

$$(EQE\ q) / (hf) = R \qquad (1)$$

q is the electron charge, f is the frequency of optical source and h the Plank constant

$$(Af)^{1/2} / (R/in) = D \qquad (2)$$

A is the active area of device, f is the electrical bandwich, R the responsivity and *in* the noise current. Detectivity and the noise equivalent power (NEP) figure of merit at 530 nm and 0V were calculated to be 1.53 10^{11} Jones and 2pW/sqrt (Hz) respectively.

Noise spectra (figure 2) show an evident bias dependence due to an increase on dark current; in particular a 1/f contribution appears for higher potential. A very small noise current (<1 pA/sqrt (Hz)) is achieved under 0V.

The dynamic response plotted with Bode diagram (figure 3-a), shows a first cut–off frequency at 42 Hz (-3 dB) and a peculiar lift starting at 400 - 1000 Hz (-10 dB), thus allowing to define a second cut-off frequency at 92 KHz (-13 dB). Distortion phenomena were monitored with eye diagram plots (Figure 3b) by square-wave modulation of the LED source at different frequencies.

Our results indicate the potential of Perovskite-based photodiodes for low cost and high performance applications.

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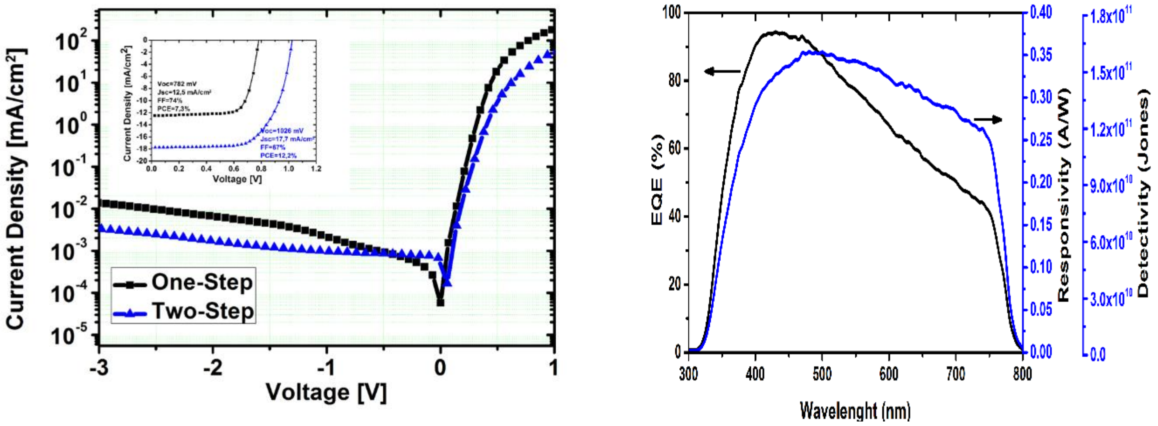

Figure 1:a) JV characteristics in dark of devices fabricated with one-step and two-step procedure. In the inset a comparison of the current density-voltage (JV) curve at 100 mW/cm2. b) EQE, Responsivity and Detectivity of device fabricated with two step deposition.

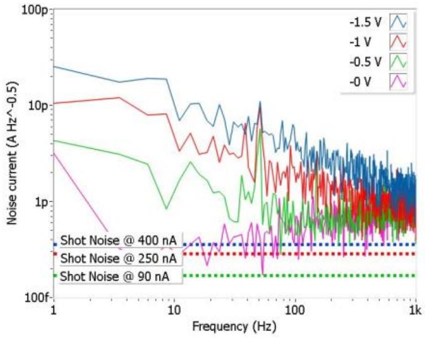

Fig. 4. Noise spectral density of the dark current at different bias. The corresponding theoretical shot noise was reported with dashed lines

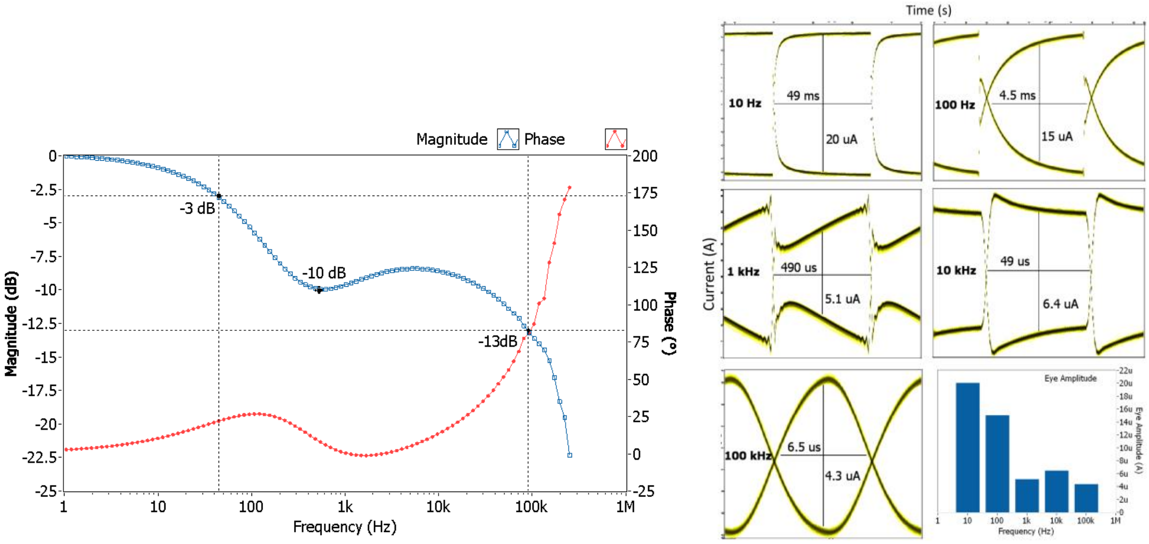

Fig. 5. a)Bode diagram (Magnitude and Phase) of device fabricated with two-step deposition associated to optical modulation (input) and photocurrent signal (output). B) Eye diagram and graph of the relation Eye amplitude-Frequency .

Simulation of HgCdTe LWIR photodetectors

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Accurate coupled electrical-optical modeling of Focal Plane Arrays (FPA) infrared (IR) detectors is essential to optimize detectivity and spectral response with respect to epitaxial composition and doping profiles. We present simulations of HgCdTe-based long wavelength infrared (LWIR) detectors, focusing on methodological comparisons between the finite difference time domain (FDTD) [1-4] and ray tracing [5] optical models. The absorbed photon distribution, photocurrent (I_{ph}) and internal quantum efficiency (IQE) of isolated pixels have been calculated to investigate the effects of light back-reflections induced by passivation coatings and metallizations, characterized by high reflectivity at IR wavelengths.

A first group of three-dimensional (3D) simulations describes the absorbed photon density distribution in single pixels of uniform composition (Figure 1), systematically comparing the results obtained with FDTD and ray tracing (Figures 2-4). Ray tracing is a classical optics approach, unable to describe interference effects, easily captured instead by FDTD. As expected, the applicability of ray tracing is found to be strongly wavelength-dependent, especially when reflection from metallic layers is relevant. I_{ph} and IQE obtained with the two methods are compared and discussed, identifying the cases where ray tracing can be considered a viable approximation.

A second group of simulations will extend the comparison between FDTD and ray tracing to graded-composition and dual-band pixels [6-8], where energy gap and refractive index are position-dependent [9].

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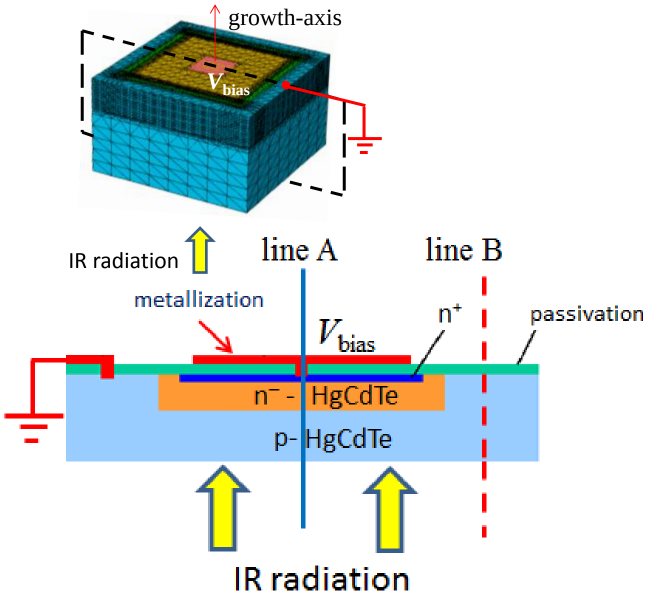

Figure 1: 3D view (above) and 2D cross section (below) of a LWIR pixel. The vertical lines (through the metallic contact, solid, and outside it, dashed) mark the cuts along which the absorbed photon density is reported in Figures 2-4.

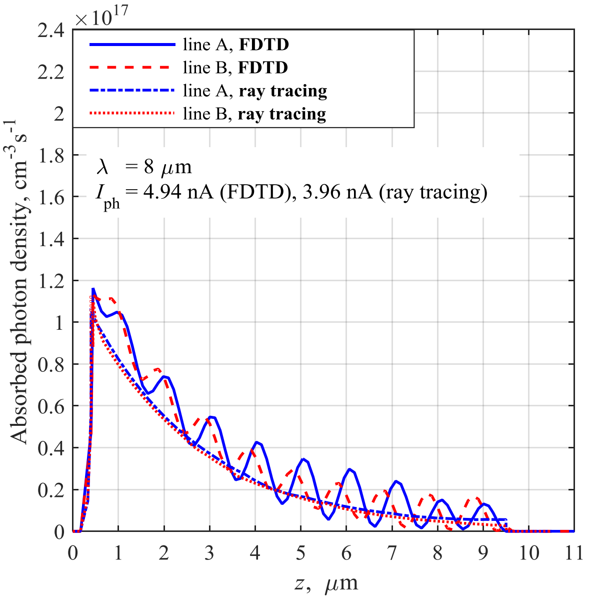

Figure 2: absorbed photon density at λ = 8 μm, along the lines shown in Figure 1, calculated with FDTD and ray tracing. The photocurrent I_{ph} calculated with the two formalisms is also reported.

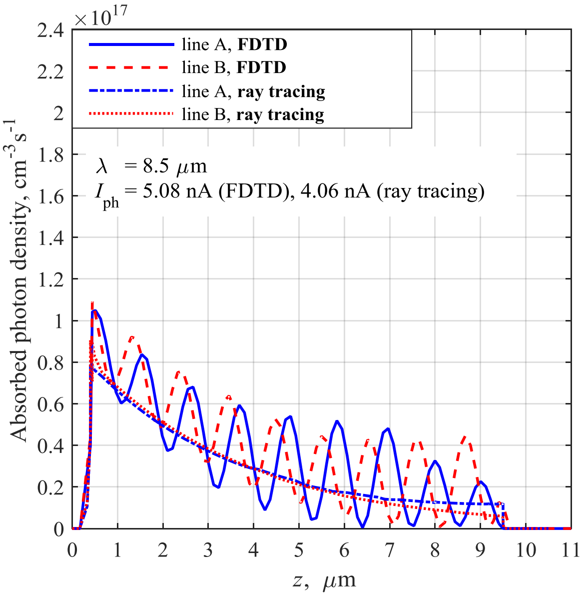

Figure 3: absorbed photon density at λ = 8.5 μm, along the lines shown in Figure 1, calculated with FDTD and ray tracing. The photocurrent I_{ph} calculated with the two formalisms is also reported.

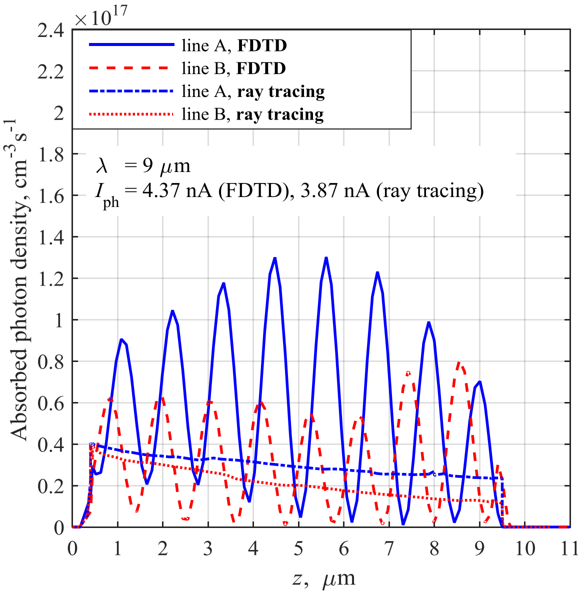

Figure 4: absorbed photon density at λ = 9 μm, along the lines shown in Figure 1, calculated with FDTD and ray tracing. The photocurrent I_{ph} calculated with the two formalisms is also reported.

Trap-assisted Tunneling in InGaN Single-QW LEDs: correlation with technological parameters

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Since their introduction in 1993 [1], light-emitting diodes (LEDs) based on InGaN/GaN quantum wells (QW) have become the most successful technology for high efficiency solid-state lighting. Although the efficiency for blue LEDs has reached very high values, III-nitride LED technology still faces two critical issues, namely efficiency droop [2] and decrease of efficiency with increasing emission wavelength, known as "green gap" [3]. While considerable research effort has been put into the study of these two problems, relatively little work has been done on device behavior at low injection current, which only recently attracted increasing attention [4,5]. Experimental and theoretical study of the LED operation at low current density at is important for the understanding of the origin of the usually very high ideality factors n_i observed experimentally. In fact, at least in single-QW devices high n_i can be explained with trap-assisted tunneling (TAT), which in turn might influence LED efficiency [6].

In this work we studied single QW current characteristics at low injection for several LEDs emitting in the blue, having different QW thicknesses and Indium concentrations. The main parameters and some measured key figures are shown in Table 1. The measured IV curves have been fitted by simulations based on the drift-diffusion model for electronic transport in combination with 8-band k·p for the confined electronic states. TAT has been implemented based on the Hurkx model [7]. This model is a modification of the conventional Shockley-Read-Hall (SRH) recombination, where the carrier emission and capture rates are increased by a field dependent enhancement factor. This is based on the idea that in a non-zero electric field the rates are enhanced due to tunneling from or to the trap state, as shown in Fig. 1.

In Fig. 2 we show the measured and fitted IV characteristics of the different devices. Two groups of devices, A and B, can be distinguished which show qualitatively distinct features. Using the Hurkx model we obtain an excellent fit, given by the red curves. Group A device can be fitted assuming TAT mediated by the Mg dopants in the AlGaN electron blocking layer, whereas group B devices are fitted by an additional deep trap in the active region. Fig. 3 shows the band diagrams and SRH rates for two examples.

Fig. 4 shows the fitting parameters (trap density and polarization relaxation) versus the mechanical energy density, and the blueshift of experimental with respect to simulated spectra and the current at peak IQE. All quantities correlate with the strain energy, and we deduce that the appearance and amount of deep traps and unexpected blueshift is related with the structures reaching the critical QW thickness t_{crit} [8].

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	t_{QW} [nm]	x_{In} [%]	λ_{peak} [nm]	EQE [%]	I_{EQE} [mA]
A1	3	15	423	40	21
A2	3	17	440	44	15
B1	3	19.5	444	41	21
B2	3	21.5	454	38	48
B3	4	19.5	451	30	170
B4	5	19.5	444	35	250

Table 1: QW thickness t_{QW}, Indium content x_{In}, peak emission wavelength at 10 mA (λ_{peak}, in nm), peak EQE and current at peak EQE (I_{EQE}, in mA) of the different devices. The first column gives the names used in this work.

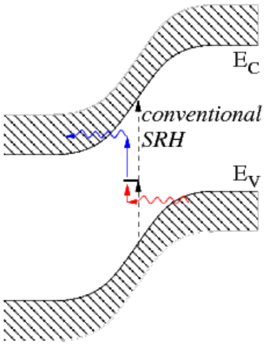

Figure 1: Schematic of trap-assisted tunneling. Carrier emission from the trap (shown for an electron) and capture (shown for a hole) are enhanced due to the possiblity of tunneling from or to the trap state. Conventional SRH process is shown with dashed arrows.

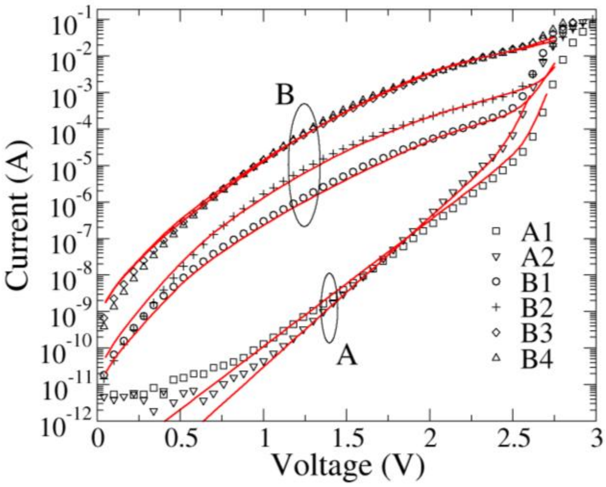

Figure 2: Measured (symbols) and simulated (red lines) IV characteristics of the five different LED structures.

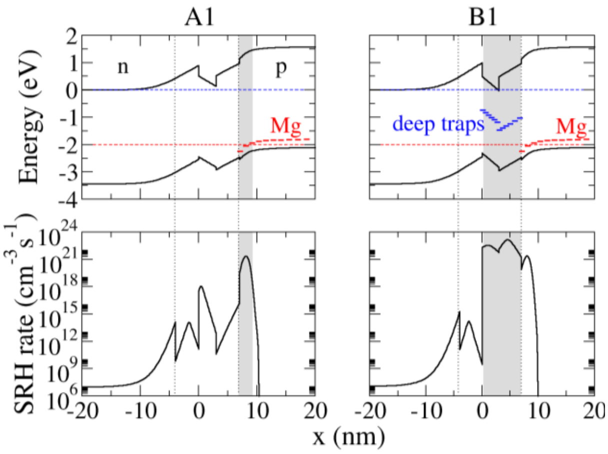

Figure 3: Band diagram (top) and trap-assisted SRH profile (bottom) for a device of group A (left) and of group B (right) at 2 V bias. Quasi Fermi levels are indicated by dashed lines. The trap states are indicated by red and blue dashes. The gray areas visualize the location of the traps mostly responsible for trap-assisted recombination current.

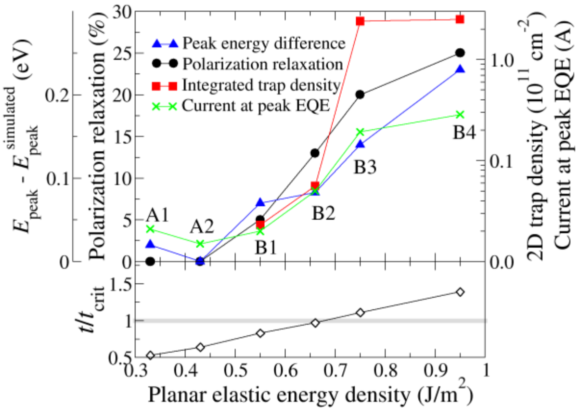

Figure 4: Fitting parameters plotted against the planar elastic energy density. The trap density (red) is given integrated across the active region, polarization relaxation (black) indicates the percentage by which theoretical polarization fields have been relaxed, and $E_{peak} - E^{simulated}_{peak}$ (blue) indicates the blueshift of measured EL spectra with respect to simulated ones without relaxing polarization fields. The current at measured peak EQE is given in green. *Lower panel*: The ratio of QW thickness to critical thickness (from [8]).

4H-SiC Power Devices Models

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Starting from recent advances in modeling of 4H-SiC VJFETs power devices [1], in the following we show its extension to analytically describe the reverse current characteristics of JBS, with blocking voltage higher than kV, and the forward curves of DMOSFET at temperature operation higher than 425K. Being physically-based, all the developed models make use of geometrical and physical quantities only and do not require fitting parameters, so that they represent an useful starting point for developing SPICE compact models.
The starting model [1] is a fully-analytical model of the reverse behavior of VJFET-structures with the topology in Fig. 1a. Since the output current of these structures depends on the voltage barrier occurring in the channel, the model is capable to describe the dependence of the voltage barrier from drain voltage and the output characteristics from V_{DS}=0V up to the blocking voltage. The accuracy of the model is proven from comparisons in Fig.2.a with ATLAS simulations of devices designed with different gate depth *(Y_G),* channel width *(X_{CH}),* thickness *(Y_{EPI})* and doping *(N_{EPI})* of epilayer*,* and with experimental data taken the literature [2] as reported in Fig.2.b.
Using the analogy with JFETs, the previous model has been extended to describe the potential barrier height, $V_{SCH/CH}$, and the J_A–V_A curves of JBS structures having the schematic in Fig. 1b. As shown in Fig. 3a, differently from JFET devices, the potential barrier of JBS strongly depends on Y_R value of recessed p^+ layers. Observing that the Y_R-dependency has never been evidenced before, the origin of the above behavior is due to the perturbation of the electric field of the Schottky junction from that located in the p^+-n junction.
By enriching the JFET model [1] with an accurate description of the traps distribution of 4H-SiC/SiO$_2$ interface, a new model of the forward characteristics of 4H-SiC DMOSFETs as in Fig.1c has been developed. The model is capable to predict the forward operation of devices in a wide range of temperature and interface traps density [3]. In particular, since the model takes into account the effects of the interface traps on the threshold voltage and channel mobility as well as their temperature dependences, its gives an accurate description of I_D-V_{GS} and I_D-V_{DS} curves in a wide range of temperatures. Comparisons in Fig. 4 with ATLAS simulations and experimental data of commercial *CREE C2M0080120D (1.2kV−80mΩ)* devices [4], performed at room temperature and *423K*, allow to validate the model.

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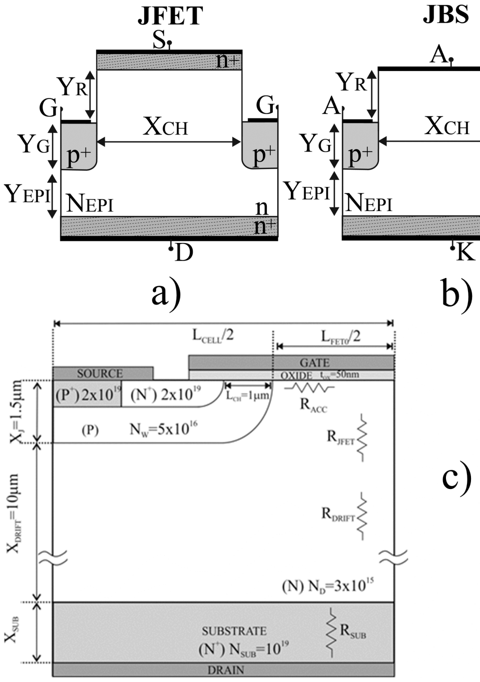

Fig.1. 4H-SiC power devices examined: a) Junction Field Effect Transistor, b) Junction Barrier Schottky, c) Metal Oxide Semiconductor FET.

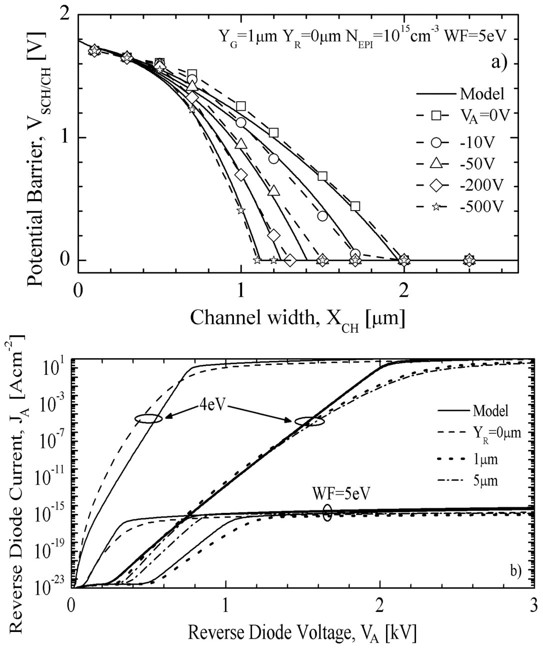

Fig.3. a) Comparison between model and simulation of the potential barrier height at different channel width for device structure in fig. 1.b at $T=300K$. b) Comparison between simulation and model of J_A-V_A curves for the structure in Fig.1.b with $N_{EPI}=10^{15}cm^{-3}$, $Y_G=X_{CH}=1\mu m$, $Y_{EPI}=15\mu m$, different Y_R and Work Function at $T=300K$.

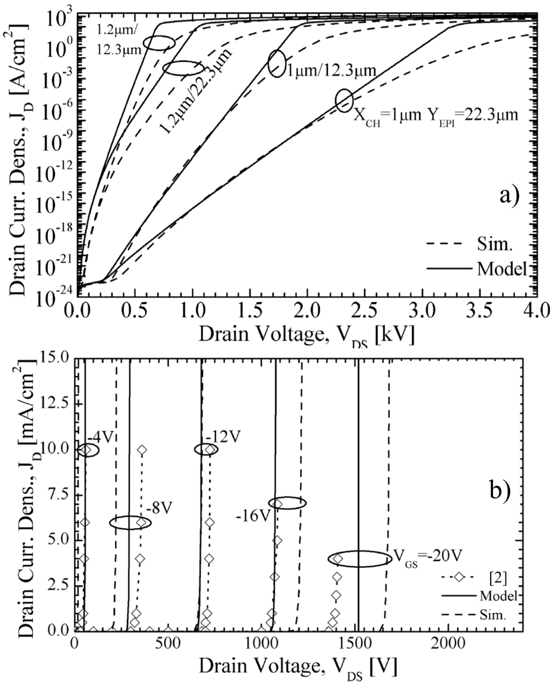

Fig.2. a) Comparison between simulation and model of J_D-V_{DS} curves for the structure in Fig.1.a with $N_{EPI}=10^{15}cm^{-3}$, $Y_G=Y_R=1\mu m$, different X_{CH} and Y_{EPI} at $V_{GS}=0V$ and $T=300K$. b) Comparison between experimental, numerical simulations and model results of [2] for different V_{GS} values and $T=300K$.

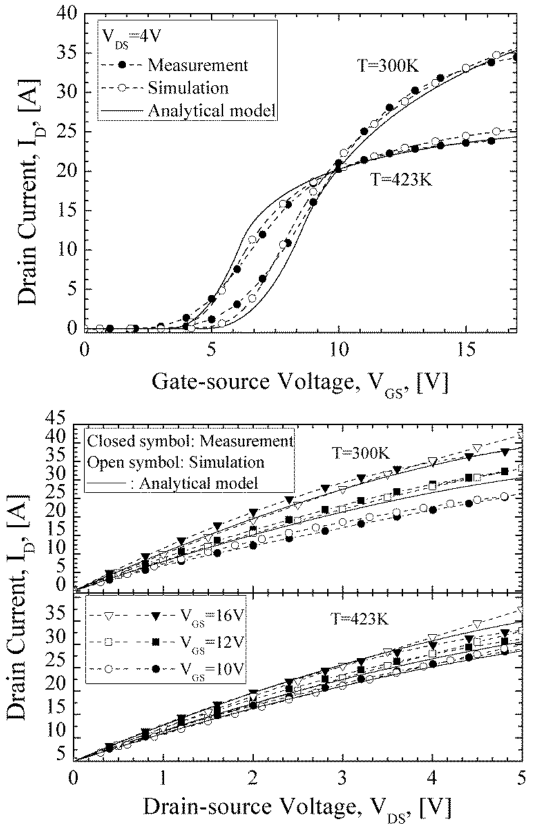

Fig.4. Comparisons of a) I_D-V_{GS} and b) I_D-V_{DS} curves between model, simulations and experimental data [4].

Analysis of impedance multiplication effects in parallel inverters

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In the last decades, renewable energy systems used for distributed generation are grown in number and importance. The increase of energy demand has led to the realization of large photovoltaic plants, with hundreds of small-paralleled inverters. The grid-connected inverters control plays an important role in system stability, especially in case of many parallel connections. In fact, parallel inverters can interact each other and bring the overall system to an unstable condition.

Fig. 1 shown, a three-phase inverter connected to a PV panel with the switches and the LCL output filters. The PV inverter has a multiloop structure, but in this work only the inner current loop is considered. The current on the inverter filter inductance L_1 is compared with a reference current, and the resulting error is the input of the current regulator. The processed error is the input for the PWM modulator, which drives the switches of the inverter.

As reported in other works, the parallel connection of inverters causes an *impedance multiplication* effect [1]. Fig. 2(a) shows that, considering the inverter output and the grid impedances, it's possible to obtain an equivalent circuit for the stability analysis, passing from a system with N-inverters to a 1-inverter system [1]. In the equivalent system the grid impedance is multiplied by the number N of paralleled inverters. The method can be applied only in case of equal inverters (equivalent in terms of output impedance), and allows knowing the impedance seen by each one. Thus, the stability from the perspective of the single inverter can be analyzed.

This work aims to consolidate some concepts linked to the *impedance multiplication effect* and weak grid condition. An instability case and a general design rule, to avoid undesired instabilities, are presented.

So far, there are many studies on PV inverter stability in weak grid case. As reported in [2]-[3], the increasing grid inductance, within a certain range, causes a lower crossing frequency in the current loop. In presence of multi-paralleled inverters, and consequently with *impedance multiplication effect*, becomes necessary an analysis for a larger range of inductances, to ensure the overall stability of the system. The phase at all frequencies below the bandwidth of the current loop must have a phase over -180°, to ensure a stable crossing at all frequencies. When the current loop control does not comply with this condition, instabilities can occur, as depicted in Fig. 3(a) for the stable condition and in Fig. 3(b) for the unstable condition.

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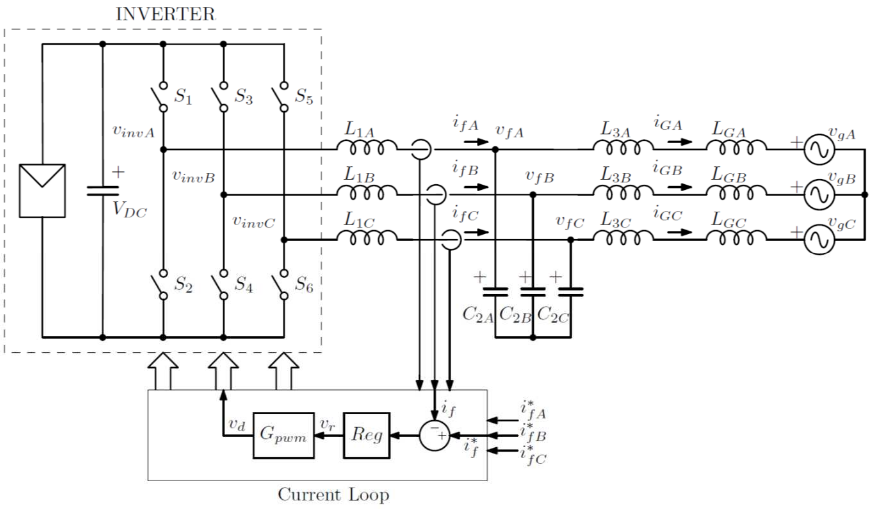
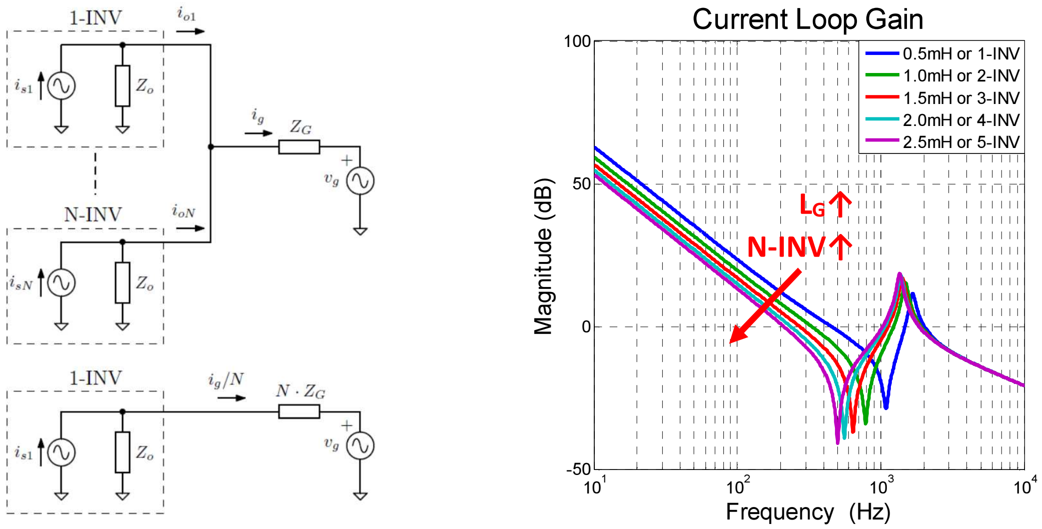


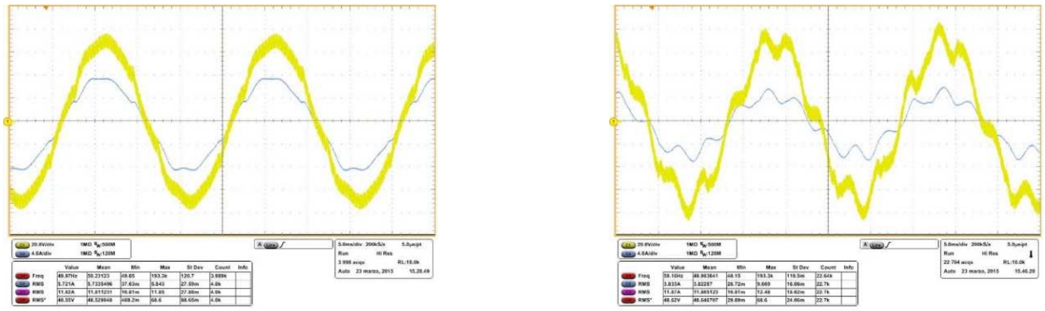
(a)

Figure 1: Three-phase inverter with PV panel, switches, DC bus, LCL output filter and grid impedance. The current loop includes a PWM modulator and a current regulator.



(a) (b)

Figure 2: (a) Two equivalent systems for the impedance-based stability analysis, N-inverters system and equivalent 1-inverter system. (b) Current loop gain with an increasing inductance.



(a) (b)

Figure 3: Output current and voltage of a 15kW 3-phase inverter: stable condition (with low grid impedance) and unstable condition (with high grid impedance).

Design aspects of a robust snubberless power converter with Si and SiC Power MOSFETs

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A number of harsh-environment high-reliability applications are undergoing substantial electrification. The converters operating in such systems need to be designed to meet both stringent performance and reliability requirements. This work focuses on a dc-dc converter for novel avionic applications and considers both new semiconductor technologies and the application of design techniques to ensure that robustness is maximized and stress levels minimized. In this respect, close attention is paid to the thermal management and an approach for the heatsink design aided by finite element modeling is shown.

As part of consistent EU activities targeting the development of more electric aircraft, higher voltage on board power distribution buses (e.g., 270 VDC) are being considered [1]. In this work, reference is made to a dual-active bridge DC-DC converter topology rated at 1.2 kW, $270V_{IN}$-$28V_{OUT}$ intended for operation at ambient temperature of 75 ºC [2,3]. Fig. 1 shows the circuit schematic; its basic operation is broadly reported in the literature [4,5]. Latest generation 650V ROHM SiC MOSFETs are used at the primary side (270 V) [6] and Infineon Opti-MOS transistors at the secondary side (28 V) [7]. Fig. 2 shows the first prototype of this converter [8].

Design for robustness

Soft-switching techniques encompass Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) methodologies. Both foresee the use of controlled resonance phenomena between inductive and capacitive elements to achieve non-dissipative turn-on or turn-off of the switching devices. Beyond, being an extremely powerful solution for improving the efficiency of switching power converters, these techniques also enable a considerable reduction of the electro-thermal stress level affecting solid-state devices and thus are an important asset in circuit design for robustness and reliability. For the present goals, only ZVS was implemented: the converter limits the resonant transition to the commutation events to realize ZVS at turn-on of the power MOSFETs.

Both transistor types used are avalanche rugged, that is, they can withstand energy dissipation in the avalanche regime enabling the design of fully-snubberless robust solutions. Whereas for low-voltage Si devices avalanche-ruggedness is achieved by design with well established and amply investigated solutions, in SiC MOSFETs this feature is associated with the material physics and has not yet been thoroughly explored. The experimental waveforms (Fig. 3) of the drain current, I_D, and drain-source voltage, V_{DS}, for unclamped inductive switching of the device shown that it can safely withstand avalanche breakdown for a drain-current value of up to more than 10 A, which is more than twice the nominal input current.

Power tests were performed on the prototype with natural and forced air convections. Indeed, in the avionic applications the converter is fan cooled in the nominal operating conditions but it must be able to operate also in case of fan failure, with 50% power derating.

Once the power losses of active and passive components are minimized by proper choice of topology, components, layout and driving, the only possible way to improve the thermal performances of the converter is the optimization of the thermal path toward the ambient. Due to the strict requirements in term of space, weight, ambient temperature, vibration and reliability, accurate 3D FEM simulation of the system is an extremely useful step for a proper design. Moreover, since the system reliability depends not only on the steady state temperature of the components but also from thermal cycles amplitude, dynamic thermal simulations are needed.

We investigate possible solutions to improve the thermal performance of the system, in particular focused on the heat-sink design, to find the best trade-off between thermal resistance and thermal capacitance. For example, Fig. 4 shows the simulation result of a solution with a finned chassis of the converter [8].

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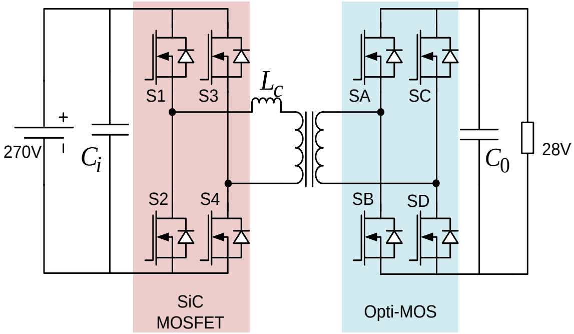

Figure 1: Schematic of the resonant-transition ZVS dual-active bridge DC-DC converter.

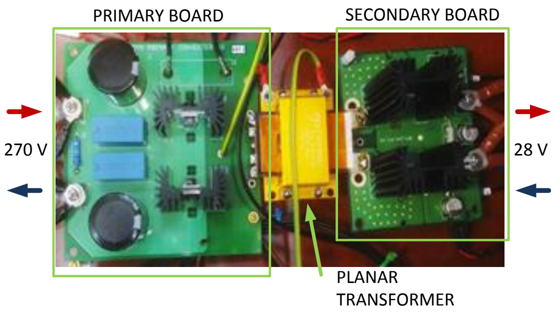

Figure 2: Top view of the prototype.

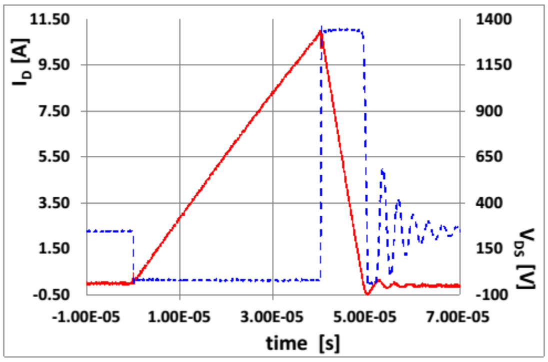

Figure 3: Representative unclamped inductive switching waveforms for a 650V SiC power MOSFET.

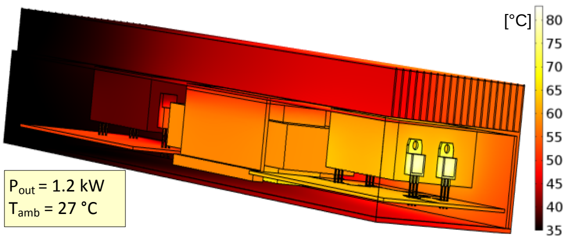

Figure 4: Finned chassis solution (secondary side to the right): simulated forced air steady-state thermal map at full load. $T_{MOSFET\_junction}$ = 83°C, T_{MOSFET_case} = 79°C.

Efficient High Step-up Topology for Renewable Energy Source Interfacing

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Some renewable energy sources, e.g. fuel cell (FC) and single photovoltaic module (PV), get to play a key role in the future distributed generation (DG) scenario. These sources present low voltage, high current output characteristics, requiring a high step-up front-end converter to transfer the available power to a high voltage DC bus in a DG architecture [1]. Among the suitable topologies, the Interleaved Boost with Coupled Inductors (IBCI) revealed to be a good candidate for PV and FC interfacing systems for the following properties: *(i)* continuous input current with low ripple [2], *(ii)* reduced switch voltage stress; *(iii)* leakage inductance exploitation, *(iv)* soft-switching in a wide load range, *(v)* soft turn-off of rectifier diodes when voltage doubler rectification is used [3].

The objective of this work is to analyze the resonant version of this topology shown in Fig. 1(a), defining the output and control characteristics, the operating modes and the optimum design criteria for the target application. The IBCI converter can be analyzed referring to the simplified equivalent representation of Fig. 1(b) where L includes the total coupled inductor leakage inductance concentrated at the secondary side, and C represents the equivalent resonant capacitance, i.e. $C_3//(C_1+C_2)$. Voltage V_A and V_B are the voltage generated by the primary switches and the secondary diodes, respectively. Analyzing the circuit all steady-state equations of interest, such as those for conversion ratios, CCM/DCM boundaries and peak transferred power, can be determined. The ratio between the switching frequency and the resonant one (the latter is that of the LC tank) influences the operating modes in which the converter can operate. If this ratio is greater than one, two continuous operating modes, CCM_0 and CCM_1, and one discontinuous mode DCM_0 are available. In Fig. 2(a) is depicted the converter waveforms in CCM_0 operating mode, while Fig. 2(c) highlights the different operating mode regions.

The design is based on the converter specifications listed in Table 1, that address the converter application as a front-end interface for a single photovoltaic module, rated around 250W (peak). The considered set of specifications allows to determine closed-form expressions for the coupled inductor turns ratio n, the energy transfer inductance L, the magnetizing inductance L_m, the clamp capacitor C_{CL} and the resonant capacitor C values. The results of the design procedure are summarized in Table 2. It's worth mentioning that the designed C value can be achieved by just reducing the $C_{1,2}$ values and removing C_3.

A prototype converter has been set up with the parameters listed in Table 1. It has been tested to validate the steady state analysis. In Fig. 2(b,c) the experimental waveforms and control characteristics, together with corresponding analysis and simulation results, are shown as example. Analytical and simulated waveforms differ only because of a non zero ripple on the clamp capacitor voltage, that was neglected in the theoretical analysis. Considering that dead times have not been modeled nor taken into account in the analysis, the experimental results have confirmed the correctness of the analytical model and of the design procedure.

The Resonant IBCI converter has an efficiency level greater than the non resonant version as the experimental measurements have showed. In fact, adding a degree of freedom due to the resonant frequency, an accurate choice of the operating mode can be done.

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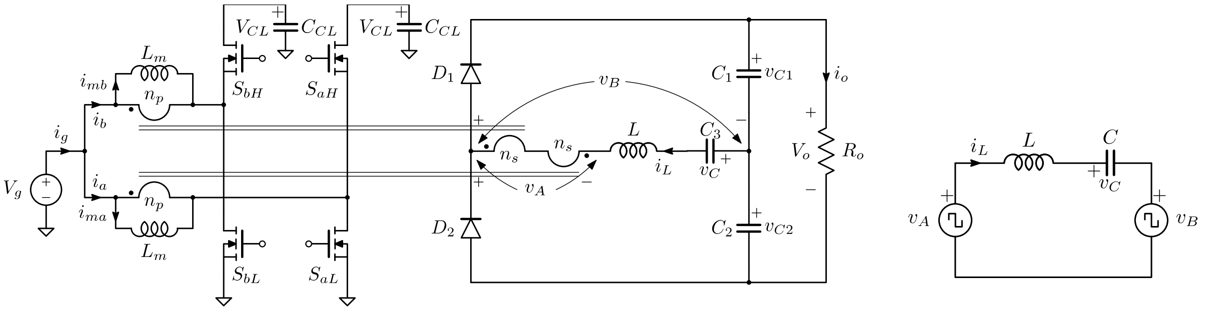
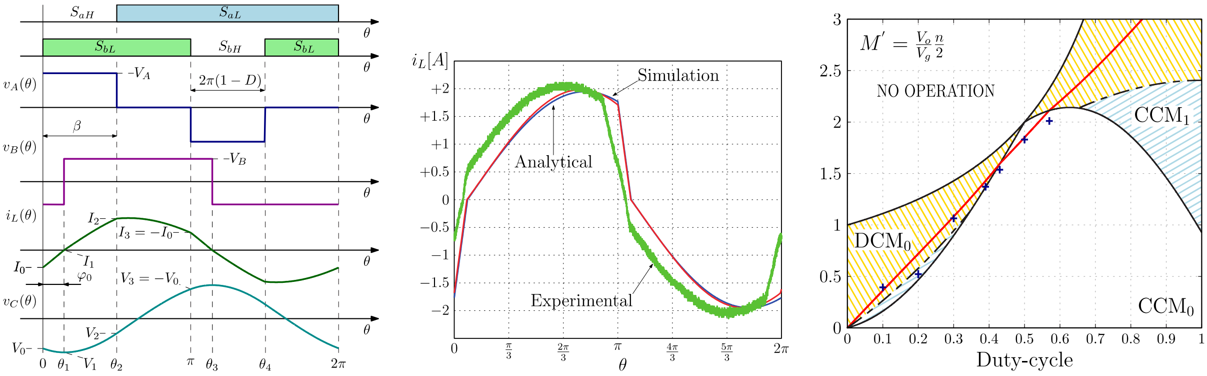


(a) (b)

Figure 1: Electrical and equivalent schemes of the considered converter: (a) Interleaved Boost with Coupled Inductor, IBCI (with voltage doubler rectifier); (b) IBCI simplified model.



(a) (b) (c)

Figure 2: (a) Main converter waveforms for *CCM_0* operation with *$D>0.5$*; (b) Measured energy transfer inductor current waveform for *CCM_0* operation at the nominal operating point, i.e. V_g = 25V, V_o = 400V, P_o = 300W: blue trace represents the analytically determined waveform, red trace is numerically simulated, green trace is experimentally measured. Measured efficiency is *95.7%*; (c) Voltage conversion ratio *M'* as a function of duty-cycle. The red, solid line corresponds to a 533Ω resistive load (i.e. to nominal power, 300W). The blue '+' indicate experimental test results.

Parameter	**Value**
Minimum input voltage	25 V
Maximum input voltage	35 V
Output voltage	400 V
Output power	300 W
Magnetizing current relative ripple	0.7
Clamp capacitors relative voltage ripple	0.1
Output capacitors relative voltage ripple	0.02
Switching frequency	200 kHz
Maximum switch voltage stress	75 V

Table 1: Converter specifications.

Parameter	**Value**
Energy transfer inductance *L*	55.6 uH
Magnetizing inductance L_m	20 uH
Turns ratio *n*	6:24
Clamp capacitors C_{CL}	470+22 nF
Output capacitors $C_{1,2}$	10+10 nF

Table 2: Converter parameters.

Experimental study about Single Event Effects Induced by Heavy Ion Irradiations in SiC Power MOSFET

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Silicon Carbide Power Devices are becoming very popular devices in switching power converters [1]. SiC devices have an epitaxial layer much thinner and more highly doped with respect to silicon devices with comparable blocking voltages [2]. The objective of this paper is to present the results of an experimental investigation about the sensitivity to Single event effects, SEE, induced by Heavy Ion irradiation in SiC power MOSFET [3-5].

We used commercially available SiC power MOSFETs which include chips with epitaxial layer thickness of about 8 µm. The devices were irradiated with ^{79}Br ions at 550 MeV, 240 MeV, 60 MeV and 20 MeV. The corresponding ionization energy losses and ranges, reported in Fig.1, have been evaluated by SRIM Monte Carlo simulations [6].

The results of Figs. 2 a) and b) refer to irradiations with ^{79}Br at 60 MeV having a range in SiC comparable to the epi-thickness. The two figures report the variations δI_{DSS} of drain leakage current and I_{GSS} gate leakage current, respectively, measured before and after irradiations performed at increasing biasing drain voltage and $V_{GS} = 0$ V. We highlight with red circles the test conditions at which the DUT failed during the irradiation. We attribute the failure to a Single Event Gate Rupture (SEGR) because of three reasons: a) there was a step increase of the I_{GSS} measured during the irradiation (see Fig. 3); b) the gate had been already partly damaged by irradiations performed at lower biasing voltage; c) The value of I_{GSS} measured after the irradiation at the critical voltage is much larger than the corresponding I_{DSS}. The devices have a similar behavior for the irradiations with ^{79}Br at 240 MeV and 550 MeV but the critical voltage is reduced to 140 V and 100 V, respectively.

Irradiation with at 20 MeV did not alter I_{DSS} and I_{GSS} measured after the irradiation up to a biasing voltage of 1000 V (see Fig. 4). During the irradiation with $V_{DS} = 1000$ V a Single Event Burnout (SEB) was observed. We identified the phenomenon as a SEB thanks to a very large drain current pulse reported in Fig. 5 a) detected during the irradiation. For comparison we report in Fig. 5 b) the typical current pulses registered during the irradiations. Furthermore, after the large peak, the leakage gate current becomes negative contrarily to what happens after a SEGR. An overall picture of the robustness of SiC power MOSFET to SEE induced by Br irradiation is reported in Fig. 6, where the failure voltage, either SEGR or SEB, are shown as a function of the energy of the impacting ions.

In conclusion we can say that SiC Power MOSFETs are less tolerant to SEGR than Silicon counterparts. Moreover, SEBs are observed in SiC MOSFETs at impacting ion energies much lower than those required to induce SEB in Silicon Power MOSFETs.

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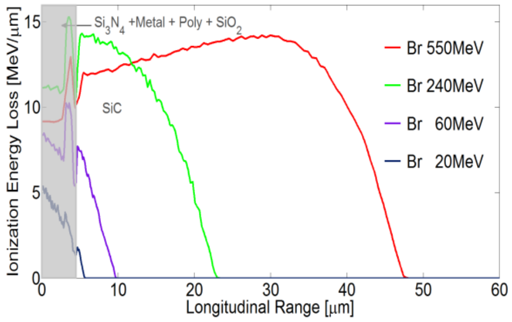


Fig.1: Energy loss vs longitudinal range.

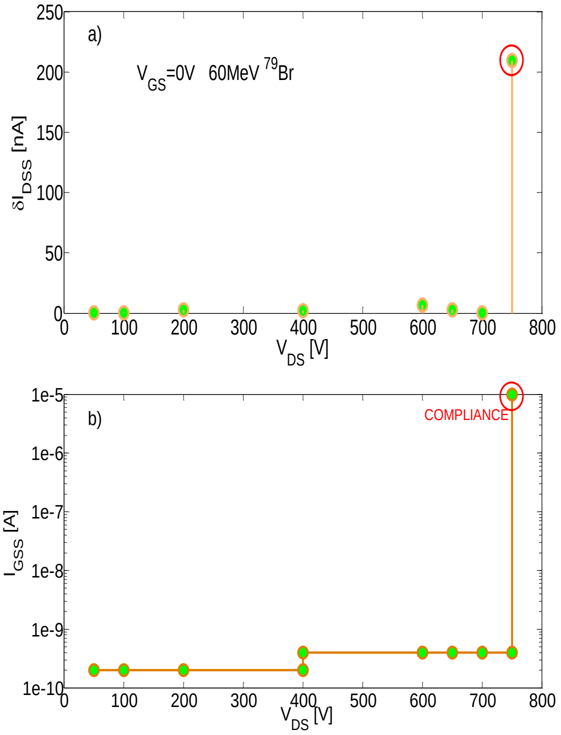


Fig.2: The variation δI_{DSS} of the drain leakage current, measured before and after irradiations with ^{79}Br at 60 MeV at increasing biasing drain voltage, vs. this biasing voltage a). The I_{GSS} measured at V_{GS}=10V after the irradiation b). The red circle highlights the irradiation which caused damage to the DUT.

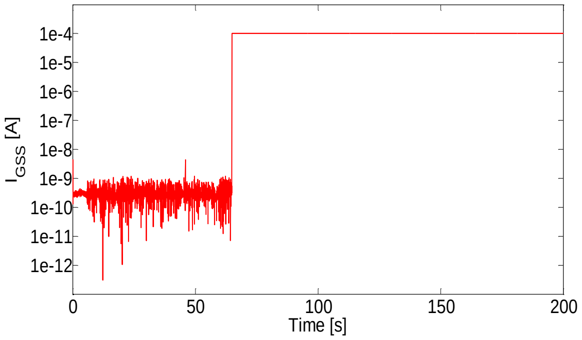


Fig.3: The I_{GSS} time evolution during the 60 MeV ^{79}Br irradiation at the test condition, V_{DS}= 750 V and V_{GS}= 0 V, where SEGR is detected.

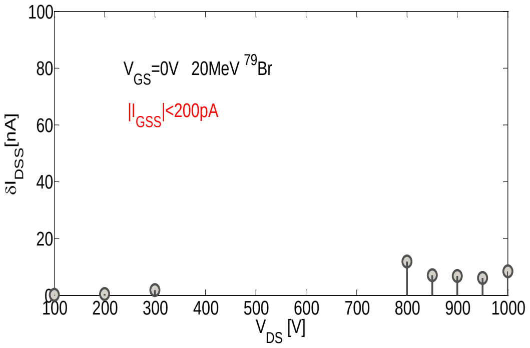
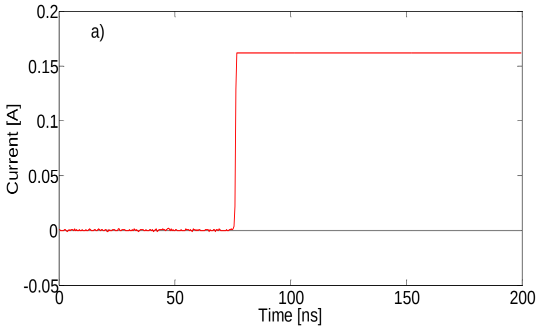


Fig.4: The variation δI_{DSS} of the drain leakage current measured before and after the irradiation with ^{79}Br at 20 MeV.



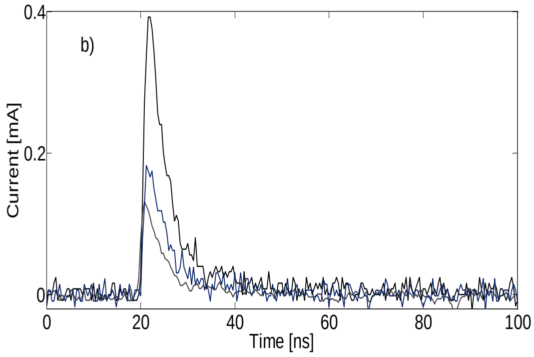


Fig.5: The current pulses recorded during the 20 MeV ^{79}Br irradiation at the test condition V_{DS}= 1000 V and V_{GS}= 0 V: the SEB pulse a); typical current pulses b).

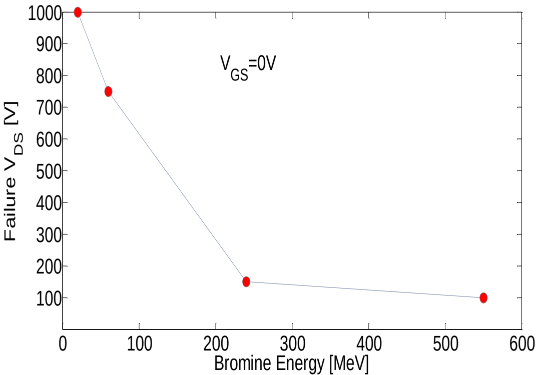


Fig.6: Failure voltage during ^{79}Br irradiations as a function of the beam energy.

NBTI reliability in power U-MOSFETs

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Introduction. With the increasing demand of renewable energy, smart and mobile low-power applications, the power devices are gaining more and more interest. Since the combined effect of large gate voltage and high temperature can cause from a slight degradation of the nominal electrical behavior to a device failure, it is very important to study, by means of accelerate stress conditions, the physical mechanisms underneath the device degradation.

Approach. In this paper, we present a combined experimental/simulation study of the negative bias temperature instability (NBTI) phenomena occurring in trench-gated p-channel power MOSFETs (Fig. 1). In Fig. 2, the threshold voltage shift induced by NBTI stress, by considering different methods, is shown. The observed degradation is function of the method adopted for the V_{TH} measurement, suggesting that when the gate-bias stress is suspended, a fast partial degradation recovery occurs [1]. In addition, the recovery mechanism is mainly linked to oxide charge de-trapping [1, 2]. In fact, by observing Fig. 3, it is possible to note the absence of the subthreshold slope and ON-resistance recovery proving hence the lack of interface states recovery. Recovery dynamics, analyzed for different recovery gate voltages (V_{G_R}), is shown in Fig.4. In particular we observe that: i) in the case of $V_{G\_R} = -2.25$ V ($V_{G\_R} \approx V_{TH}$ after stress) the V_{TH} recovery is negligible; ii) decreasing $|V_{G\_R}|$, hence moving from V_{TH} to flat band voltage (V_{FB}), a larger recovery occurs; iii) for V_{G_R} ranging from -0.25 V to 0 V no additional recovery is observed. The gate voltage dependence is explained by the energy distribution of traps. In fact, traps having energy above the channel potential (Fermi level at SiO_2/Si interface) are filled with holes and are not discharged during recovery phase. On the other hand, traps below the channel potential are discharged, leading to a recovery of V_{TH}. A calibrated TCAD sample has been simulated [3], taking into account the trapped oxide charge density ΔN_{OT} extracted from the experimental ΔV_{TH}. As a result, by reproducing the experimental conditions, oxide traps involved in the recovery mechanism show an energy confined in the range of 0.22÷0.84 eV from silicon valence band [4]. Moreover, an estimation of the spatial position has been performed by means of the tunneling time constant model [5, 6]. In order to calculate the oxide traps distance (x) from SiO_2/Si interface, we have modeled the dynamic of V_{TH} recovery, shown in Fig. 5 [4]. As a result, a model with different time constants is needed, suggesting different depth of the oxide traps. By considering the smallest and the largest time constant in the energy range of (0.22-0.84) eV, the possible physical locations of the traps, extracted by tunneling time constant model, are reported in Fig.6.

Conclusions. Stress and recovery phase have been analyzed in different conditions in order to understand which mechanisms are responsible for the NBTI degradation. In particular, by adopting different methods for evaluating the V_{TH} degradation, we found out that when the gate-bias stress is suspended, a fast partial degradation recovery occurs. Finally, it has been shown that the recovery mechanism is mainly linked to oxide traps having an energy confined in the silicon band-gap and a distance from SiO_2/Si interface between 2.24 and 3.05 nm.

Acknowledgements. The authors wish to thank the IMS-R&D NPDD Group of STMicroelectronics Catania for providing the samples and for the useful discussions.

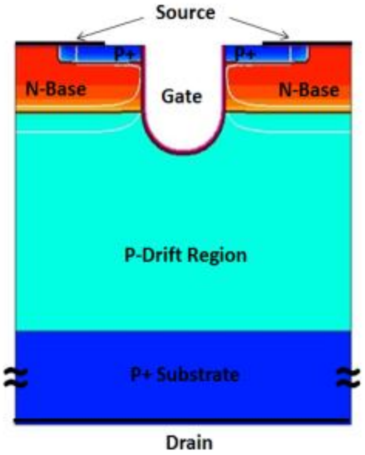

Fig. 1. A schematic of the trench p-channel power MOSFET (not in scale) realized on-wafer by STMicroelectronics and implemented in the TCAD simulator.

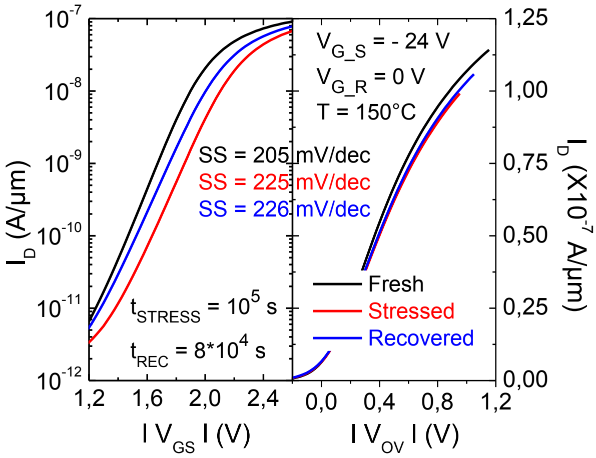

Fig. 3. Drain current curve in fresh, stressed and recovered devices, in logarithmic (left) and linear scale (right). After the recovery phase we observe a significant V_{TH} recovery whereas the mobility recovery is negligible [1, 2].

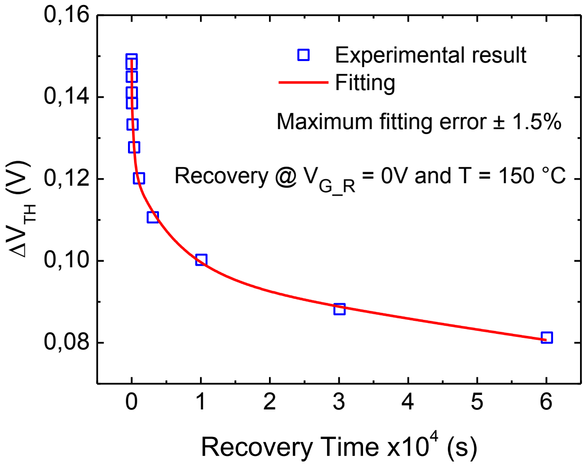

Fig. 5. Experimental (markers) and fitted (line), with (3), threshold voltage shift versus recovery time for VG = 0V and T = 150°C. [4]

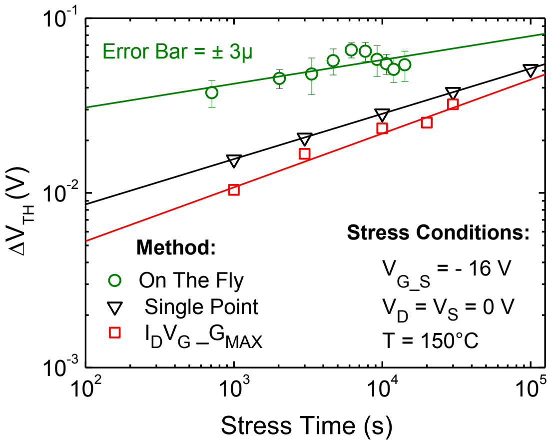

Fig. 2. V_{TH} shift induced by NBTI as a function of the stress time. Different methods are implemented for the V_{TH} evaluation. Because of the different measurement time, different shifts are estimated due to the recovery happening during the measuring phase [1].

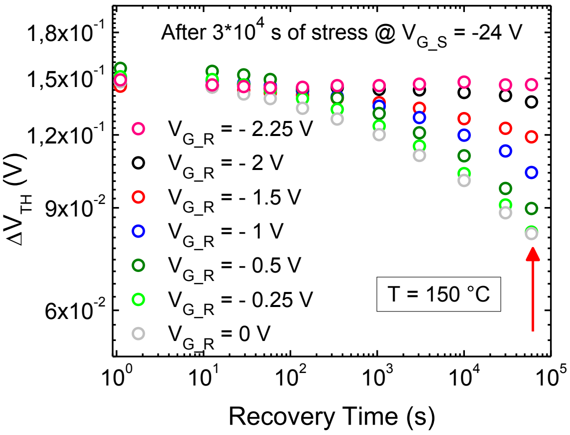

Fig. 4. V_{TH} recovery for different recovery biases. The gate voltage dependence is explained by the energy distribution of traps. [4]

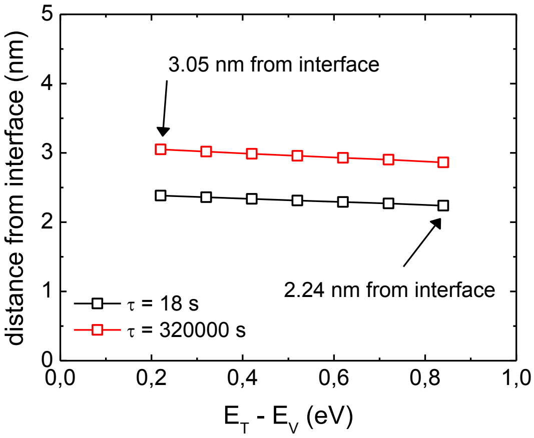

Fig. 6. Distance of the oxide traps from SiO_2/Si interface vs. trap energy level. The distance of traps from interface has been estimated as 2.24 and 3.05 nm. by considering the smallest and largest time constant, respectively [4].

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Qi-ready, Cortex-M0 based, wireless power charger for low-power, wearable devices

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Wireless Power Charger technology experienced a growing interest in recent years and some of the largest electronics component manufacturers propose their own reference design based on dedicated chip. One of the leading proposer of wireless power transfer technology is the Wireless Power Consortium (WPC), which describes the Qi-standard interface definition [1]. Qi-standard devices achieve high efficiency in wireless energy transfer by means of resonance coupled, magnetically aligned planar coils [1]. The wireless charging technology is suitable for portable and mobile application in which a galvanically insulated package is required for safety reasons, such as in biomedical or fitness devices [2].

The proposed system has been designed with an entry-level microcontroller unit, provided by STMicroelectronics. The STM32F0 is a Cortex-M0 microcontroller with very low-power consumption, very reach peripheral portfolio and a CPU that runs up to 48 MHz. These microcontrollers feature the performance required to achieve a wireless power charger implementing the Wireless Power Consortium Qi-specification.

Fig. 1 depicts the block diagram of the system, which is composed by a microcontroller, a high-frequency power inverter and a current/voltage sensing section.

The power inverter section consists of a couple of n-channel MOSFET (STL6N3LLH6) in half-bridge configuration driven by a high-frequency bridge driver (L6747A), as depicted in the schematics of Fig. 3. The bridge driver ensures an extremely fast turn-on of power MOSFETs, avoiding cross-conduction effect thus maximizing the overall inverter efficiency. The power section is powered directly by the 5 V USB voltage and can sunk up to 500 mA compliancy with the USB current rating. Lastly, the n-channel half-bridge inverter drives the LC resonant tank (the transmitting coil and a resonance capacitor), tuned at a frequency of 120 kHz. The microcontroller can vary the half-bridge switching frequency in the range of 110 kHz – 205 kHz accordingly with the required output power. A lower switching frequency corresponds to a higher transmitted power.

As described by the Qi-specification, a power receiver communicates information of required power, modulating the transmitter power carrier with the load modulation technique, affecting the system in terms of voltage and current variation into the primary coil [3]. The developed power transmitter is able to demodulate the stream of bits sent back by power receivers by means of a fully-digital synchronous peak envelope detector, which operates by sampling the power carrier’s peaks synchronously with the inverter switching frequency. As illustrated in schematics of Fig. 3, only a simple protection Op-Amp buffer is placed between the power carrier section and the microcontroller’s ADC, and a third-order IIR digital filter extracts the stream of bits from the carrier envelope.

This work proves that a Qi-compatible, very cheap Wireless Power Transmitter can be achieved, without using any dedicated chip. Moreover, the mean power consumption during stand-by is less than 30 mW and the overall power transfer efficiency can be as high as 70% [3].

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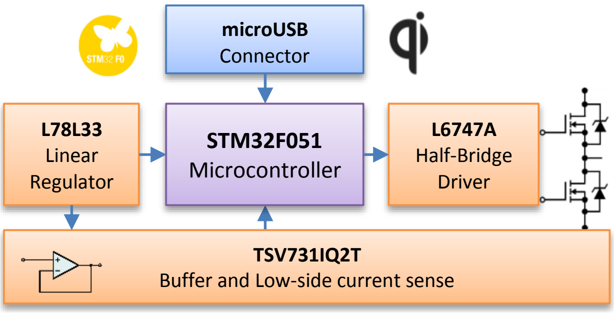

Figure 1: STM32F0 Wireless Power Transmitter block diagram.

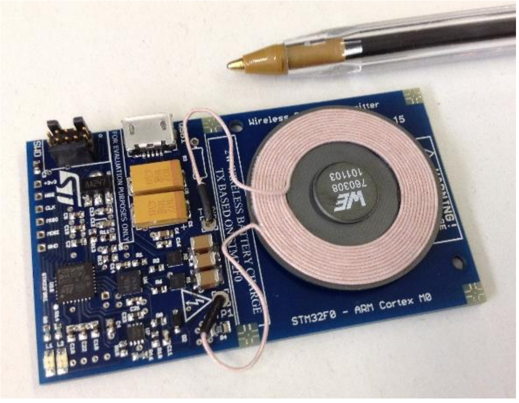

Figure 2: Picture of the developed Wireless Power Charger with the 6.5 µH Wurth coil.

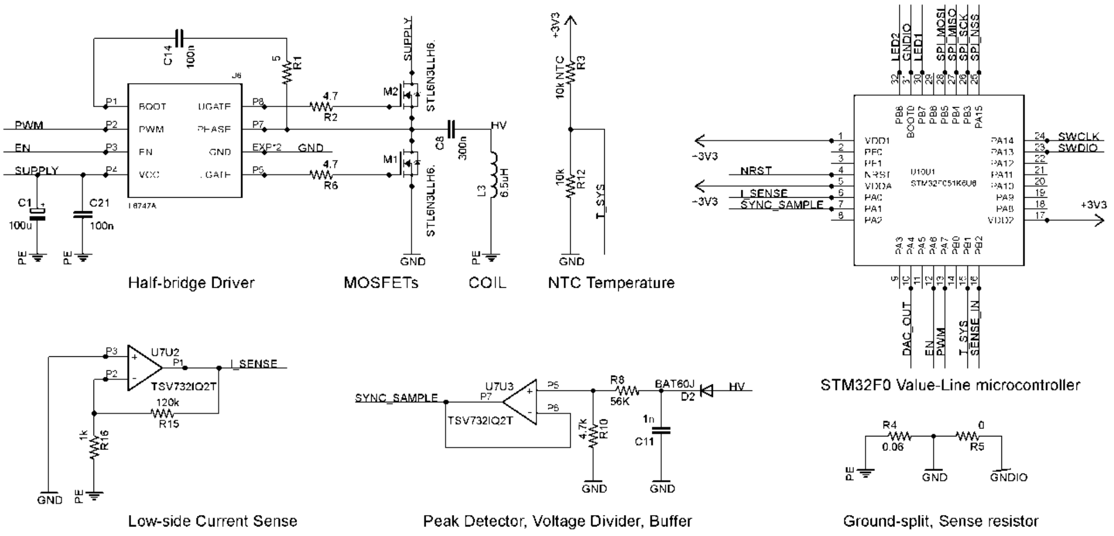

Figure 3: Wireless Power Transmitter schematics. This schematics depicts that few commercial components are needed to realize a Qi-ready Wireless Power Transmitter.

SPICE modelling of a complete photovoltaic system based on a multilevel inverter

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A SPICE model of a complete photovoltaic (PV) system, including a detailed model of photovoltaic cells, a multilevel inverter, and energy storage elements, is presented (Fig. 1). The simulation of the system as a whole yields useful information in terms of efficiency, distribution of power dissipation and allows evaluating the effects of the variation of the component parameters, such as MOSFETs and capacitors, and external parameters, such as the load, the solar irradiation, and the temperature.

The structure of the PV system used in this study includes a multilevel inverter with the Multi-cell Modified Cascade H-bridge configuration in conjunction with the Selective Harmonic Elimination (SHE) modulation technique.

A multilevel inverter is particularly suited for PV systems because the multiple DC sources required for these topologies can be obtained connecting the proper number of PV cells in series. It is also characterised by the lower switching speed of the solid state switching elements that turns into less stressed devices and therefore into an improvement of the reliability, a higher efficiency, a low dV/dt, lower electro-magnetic interferences (EMI) and a lower harmonic content in the output waveform [1], [2]. Storage elements (e.g. capacitors) are required to avoid loss of efficiency with the multilevel approach. The Multi-cell Modified Cascade inverter [3], [4], used for this work consists of the series connection of n DC blocks, allowing to obtain a $2n + 1$ levels output waveform. Among the different modulation techniques that can be used to control a multilevel inverter, the SHE method minimizes the total harmonic distortion (THD) of the output waveform by cancelling the low frequency harmonics, keeping the efficiency high and allowing to use smaller filters [5].

The PV strings in the system are composed of the series of several PV cells modelled with the double-diode exponential model [6]. An iterative method fitting the I–V solar cell characteristic has been used to find the appropriate coefficients of the model. The simulation results are compared with experimental measurements for different values of the irradiance and temperature. The use of PV cells as power generators allows to obtain realistic simulation results compared with those provided by more simple DC voltage sources.

The global conversion efficiency and the THD of the output waveform have been analysed. The role and sizing criteria of storage elements, such as capacitors, placed at the PV module outputs are also analysed for various operating conditions in order to assess their effect on the system general behaviour. The results are summarised in Fig. 2, and show that the presence of a properly sized storage capacitor is fundamental for the correct operation of the PV system, to maximise the conversion efficiency, and to minimize the distortion of the output waveform. Experimental tests have been carried out on a custom designed prototype photovoltaic system (Fig. 3) and compared to those obtained with the simulation model (Fig. 4).

The model allows the characterization of the system dynamics, given the solar irradiance, the temperature, the storage capacitance, and the AC load. It can be used for example to evaluate the harmonic content of the output waveform and to study the behaviour at the same time of the overall system and its sub-components. Efficiency, power dissipation of each element, and power generated by the photovoltaic modules, for different values of the storage elements and in presence e.g. of temperature or load variations can be evaluated.

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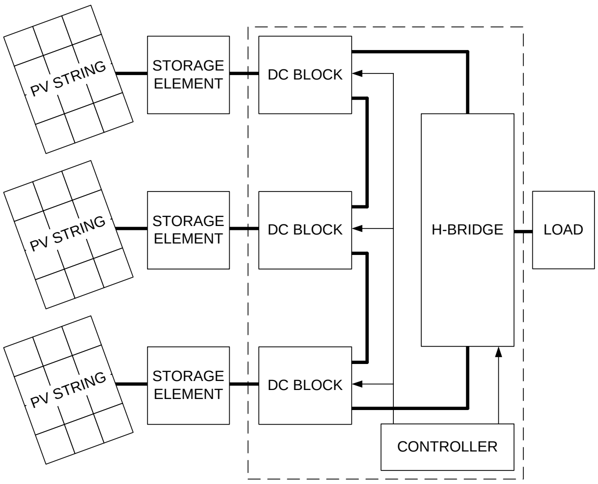

Figure 1: Schematic diagram of the simulated system.

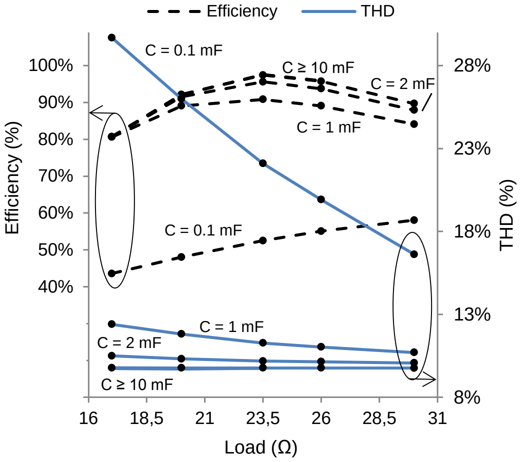

Fig. 2. Efficiency of the system and THD of the output waveform vs. load for different sizes of storage capacitors.

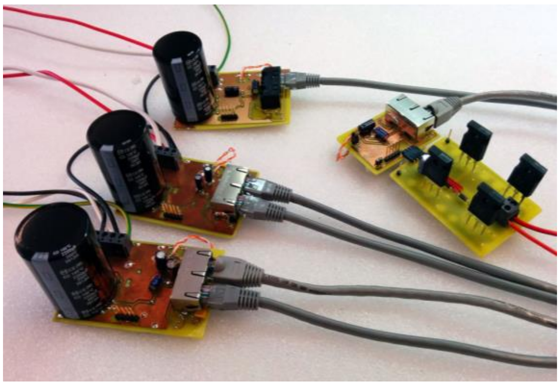

Fig. 3. A picture of the realised multilevel inverter. On the left there are the DC blocks and on the right the H-bridge and the master board.

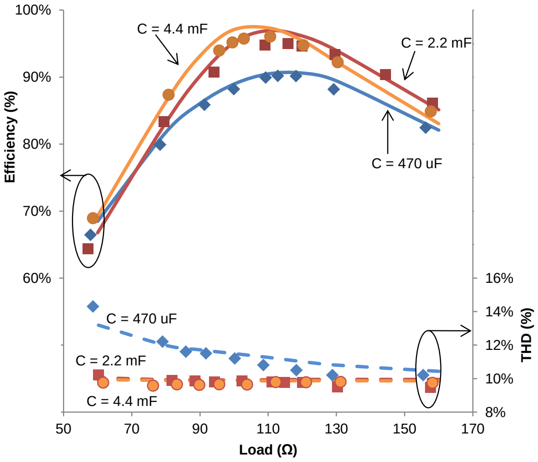

Fig. 4. Comparison of the system efficiency and THD obtained by simulations (lines) and measurements (symbols) for different loads and storage capacitors.

A device for robust measurement of biospecies in aqueous media

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Recent achievements in the field of organic bioelectronics have led to the development of biological sensing platforms and portable analytical devices such as, for instance, DNA and protein sensors. A critical requirement for these devices is the stability in aqueous media. However, a long time immersion in buffer solution [1] or a mechanical stress such as a flow of a buffer solution [2] could produce a variation in the output signal of the sensor which could be misinterpreted if, at the same time, an analyte is added to the sensing environment.

The proposed device is an Organic based Charge-Modulated Field-Effect Transistor (OCMFET) [3] suitable for the detection of charged molecules in aqueous media. Figure 1 shows a cross section of this device. The OCMFET is basically a sensor for the electric charge immobilized on the sensing area, which determines a shift in the threshold voltage of the OTFT. We demonstrated that, by means of a new functionalization method of gold surfaces through the electroreduction of aryldiazonium salts in ionic liquid, it allows to flow buffer solution over the surface without output signal variation that could interfere with actual measurement.

Figure 2 compares the OCMFET response to four flows of buffer solutions in a device in which the sensing area has been modified with this technique (b) and a reference with an un-functionalized surface (a).

Furthermore, we have demonstrated that is possible to use this functionalization technique for DNA molecules immobilization over a gold electrode and figure 3 shows an example of transfer characteristics for the OCMFET. In the case of DNA hybridization, as the model predicts, the negative groups of phosphate groups of DNA strands induce a charge redistribution in the floating gate, thus leading to a positive charge accumulation in the channel of the organic semiconductor. Using a p-type semiconductor, an increase of the output current for a given value of gate voltage is obtained. Figure 4 clearly shows that a real-time measurement of DNA hybridization is achievable, without the noise related to the flow of buffer solution.

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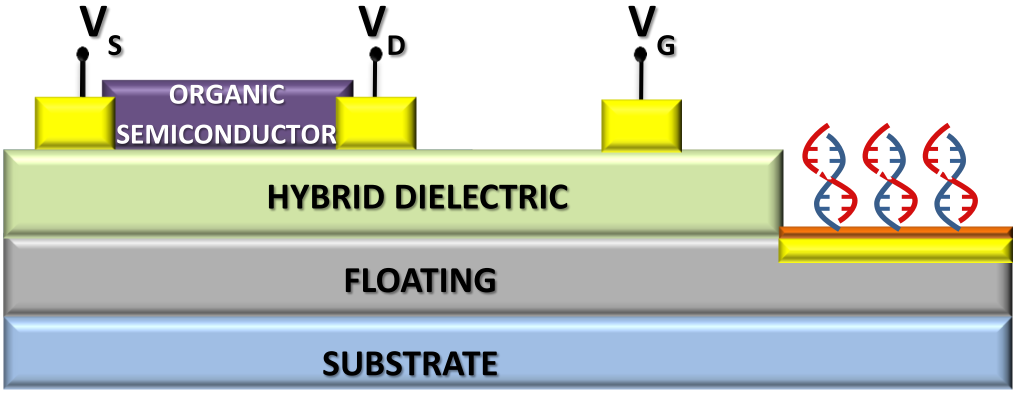


Figure 1: OCMFET structure.

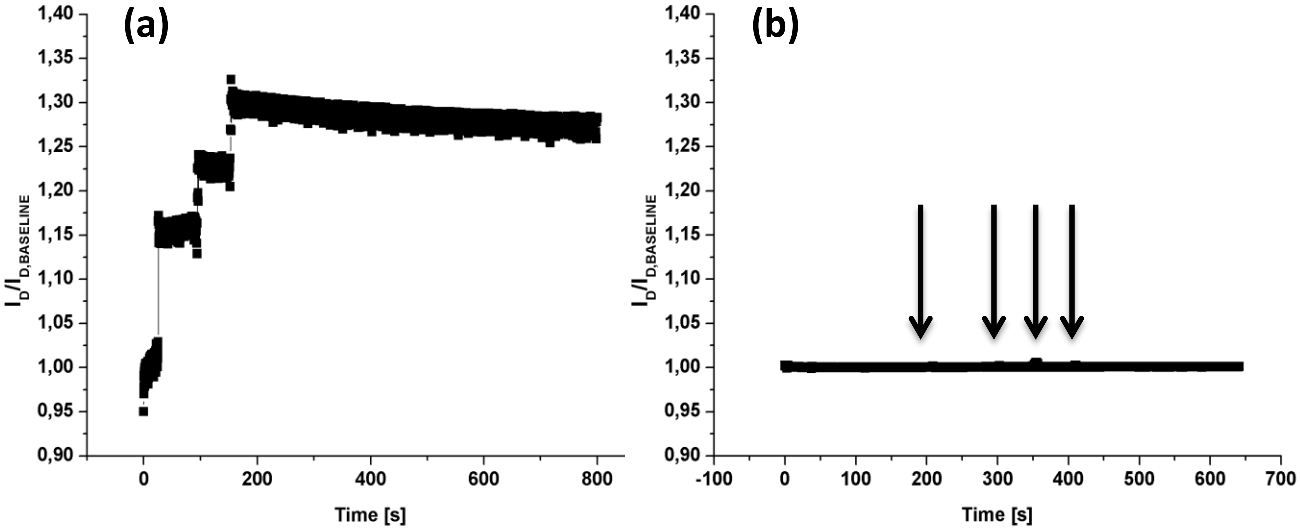
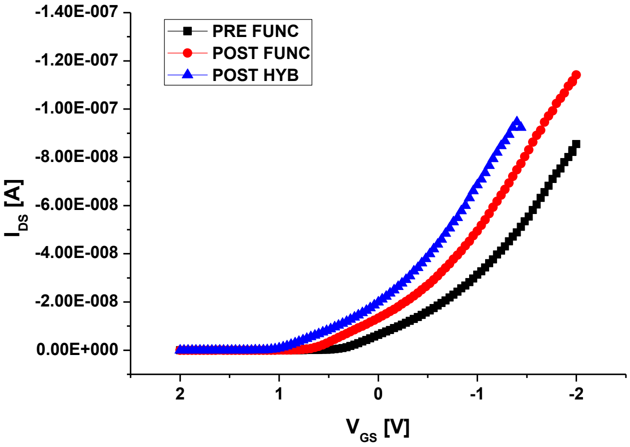


Figure 2: drain current of an OCMFET with an active electrode modified with this technique (b) and a reference device with an un-functionalized surface (a).



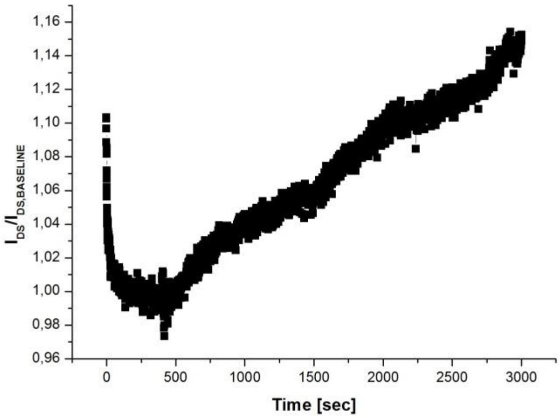


Figure 3: OCMFET transfer characteristic.

Figure 4: real time DNA hybridization detection.

A new generation of ultrasonic transducers for guided-waves inspections

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Ultrasonic Guided Waves (GW) inspection is a popular methodology employed by many Structural Health Monitoring (SHM) systems. GW inspection is typically achieved through phased arrays featuring a large number of piezoelectric transducers. The weight penalty, the complex circuitry, and maintenance concerns associated with wiring a large number of transducers have to be addressed for widespread field deployment of SHM systems.

Drastic hardware simplification and cost reduction of Guided wave (GWs) based systems can be achieved by using transducers that present inherent directional capabilities when generating and sensing elastic waves. Such capabilities can be achieved by patterning the piezoelectric material lay-out, i.e. the load distribution [1]. In particular, Frequency steerable acoustic transducers (FSATs) are based on a spatial filtering effect which is frequency-dependent, so that a direct relationship can be established between the direction of propagation and the spectral content of the transmitted/received differential signals. Arbitrary directional scanning within the [0°; 180°] angular range was demonstrated with FSATs in a recent work [2]. However, in the first practical realizations of FSATs, two main limitations appeared: i) waves are excited or sensed contemporarily in one direction and in the opposite direction (180° ambiguity), ii) just a relatively rude approximation of the desired directivity has been achieved, resulting in a wave generation/detection even in directions other than the desired one.

In this work, a new generation of FSATs is proposed, which allows to overcome the above mentioned limitations. A sample geometry of the new generation FSAT is depicted in Fig. 1. In particular, the 180° ambiguity is eliminated by combining the information of 2 differential signals rather than one [3], as happened for the 1st generation FSATs. The result of this combination is a signal whose spectrum peaks at a frequency “f_d”. The piezoelectric load distribution of the 2nd generation FSAT is designed so that the value of “f_d” varies as a function of the wave direction of propagation in the whole angular range [0°; 360°], as can be seen in Fig.2. The proposed embedded system allows to operate on composite panels tackling anisotropic and dispersive propagation, and to implement a SHM system with lower weight and size w.r.t. the actual monitoring systems. The effectiveness of the novel transducer technology is shown through a numerical and experimental validation with application to defect monitoring in an Aluminum plate.

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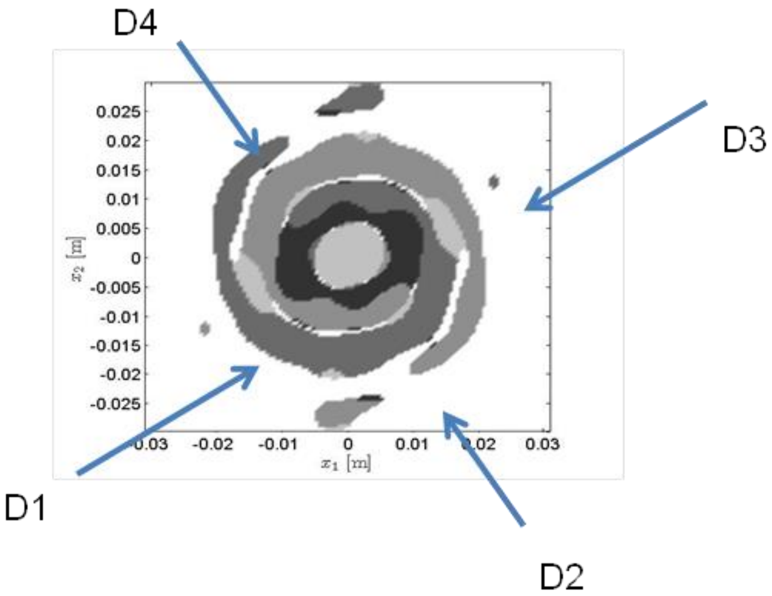

Figure 1: Sample shape of the piezoelectric transducer. The transducer electrode patches are displayed in different shades of gray. D[1-4] are the 4 different directions of propagation considered in Figure 2.

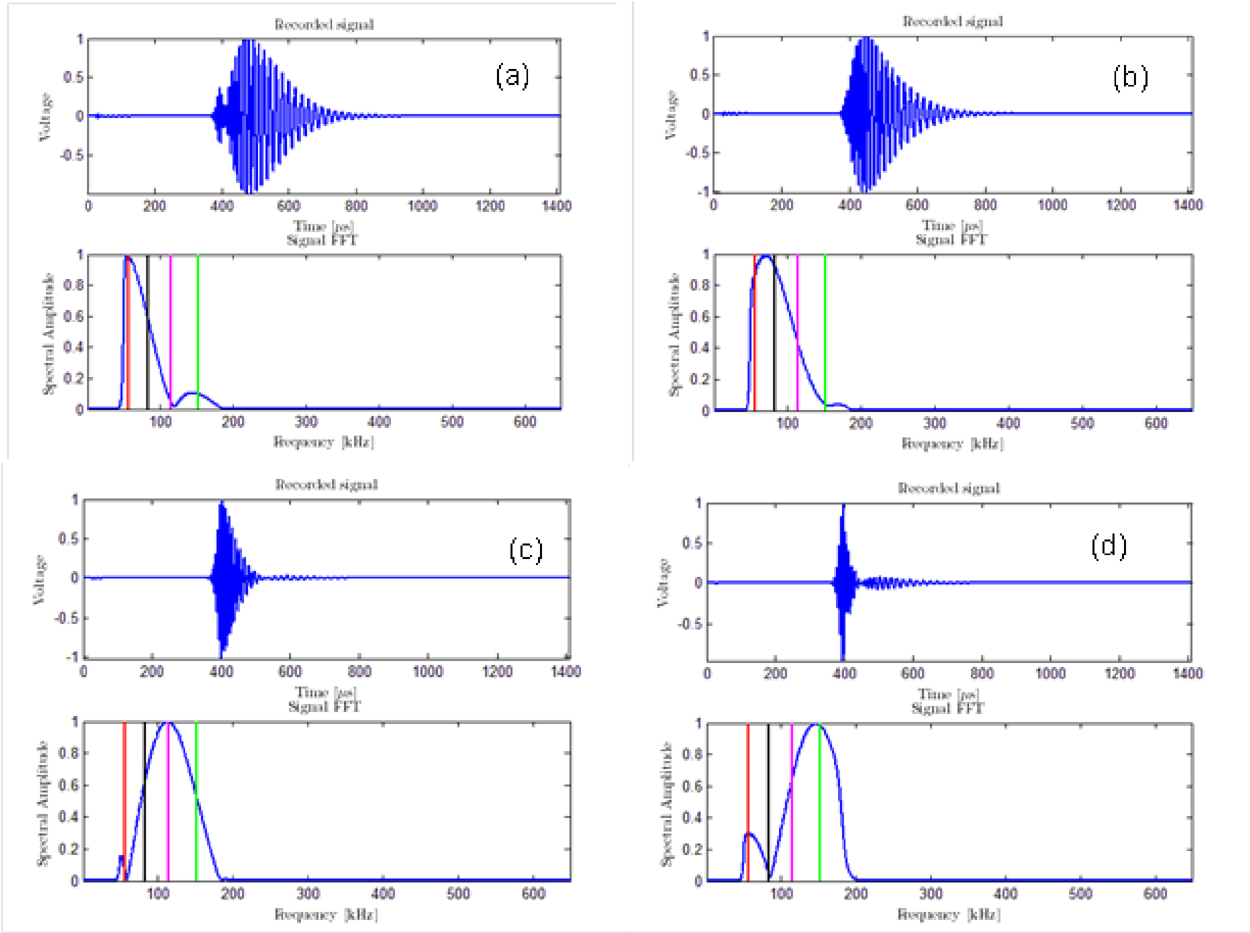

Figure 2: Pulse and frequency responses of the FSAT transducer of Fig. 1, when excited by elastic waves traveling along directions D1, D2, D3 and D4, in subfigures (a), (b), (c) and (d), respectively. The vertical lines represent the nominal peak position imposed by the implemented transducer design procedure.

Analyzing Pyroelectric emission from –Z surface of $LiNbO_3$ by integrating Microheaters

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Abstract:

Pyroelectric effect is the capability of certain crystal to produce temporary voltage during heating or cooling transient. Here we investigate the pyroelectric effect using microheaters fabricated on +Z surface of LiNbO3 crystal. Different geometries of microheaters, such as Fan, Meander, Double Spiral and S- Shape were fabricated on one side of a single domain LiNbO3 crystal, since microheaters gives an advantage of confined temperature gradient, together with low power consumption for application-based sensors [1]. In this paper, we study the electron emission from the pyroelectric material (LiNbO3), relevant to the microheaters fabricated on the crystal and also demonstrating the Pyro electro hydrodynamic (PED) effect on liquid droplet. Fabrication of the four different designs was performed in three-step process: photolithography, thin film deposition and lift off process. Titanium was the choice of heater material due to its property of forming a thin oxide layer making it a non-corrosive material for the microheaters [2].

Thermal behaviors of these microheaters were simulated using COMSOL™ Multiphysics and compared with the experimental data obtained by FLIR SC7000 Series thermo camera. Static and time-dependent thermal analyses were performed using a voltage generator by applying DC and step voltage signals to the microheater.

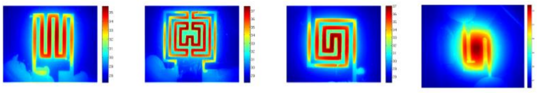

Fig1: Microheater's design (from left to right) Meander, Fan, Spiral, S shape.

It was observed that the electric field resulting from the temperature induced by the microheater changes the spontaneous polarization of the LiNbO3 crystal affecting the electron emission. This pyroelectric electron emission (PEE) from –Z surface of LiNbO3 crystal was investigated using two-probe point measurement. It was observed that the PEE from LiNbO3 is due to the perturbation, by the temperature variation, of equilibrium between spontaneous polarizations P_S in the crystal and external screening charges (q_{SC}) on its surfaces. At equilibrium, all P_S are fully screened by q_{SC} and no external electric field exists. Any excess or lack of screening charges (q_{SC}) relatively to P_S, leads to the appearance of an electrostatic state from the uncompensated charges (ρ) given by [3]:

$$\rho = \Delta\,(P_S - q_{SC}) \qquad (1)$$

Furthermore, we verified the pyroelectric emission effect in a transient condition for all the microheaters. We also verified the pyroelectric emission effect in a transient condition for all microheaters. A voltage signal was applied to the microheaters using signal generator. A tip (diameter~0.254mm) was positioned at different distances (100um-1mm) on the -Z surface of $LiNbO_3$ crystal. The current peaks acquired using oscilloscope were due to the dielectric breakdown of the air between the receiver point probe and the -Z surface of $LiNbO_3$. A gap spacing analysis between the receiver point probe and -Z surface of $LiNbO_3$ was also performed. It was also noted that the temporal distances between adjacent electrical peaks exponentially increases during the application of the thermal transient, showing a dependency of the rate of heating and cooling on the PEE in a transient condition of the crystal.

Finally, we report on an Pyro- jetting of liquid droplet from a liquid reservoir [4,5]. The PED effect was demonstrated using liquid samples of Oil, OIR-906, water and PDMS.

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Acknowledgement:

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Autonomous Sensors Powered by Energy Harvesting from von Karman Vortices in Airflow

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In this paper an innovative energy harvesting system based on a piezoelectric converter to extract energy from airflow and use it to power autonomous sensors is presented. Harvesting energy from Von Karman vortices can be effective since they are common behind obstacles in a flow [1,2]. The converter is embedded as a part of a flexure beam that is put into vibrations by the vortices detached from a bluff body placed upstream. As shown in Fig.1, a parallelepiped-shaped obstacle, with a width W, placed in a low-velocity wind tunnel has been used. The beam has been placed in the vortex street to allow periodic excitation. The beam is composed of the piezoelectric converter and a blade profile. The converter is a bimorph piezoelectric element, WAC3X/18, based on a steel slat, clamped at one end to obtain a cantilever structure. The blade has been connected to the free end of the converter to collect the vortices. Different air flows have been generated while the open-circuit voltage V_P of the converter has been measured. Fig. 2 and Fig. 3 show the comparison between the voltages V_P and corresponding frequency spectra measured for three different flow velocities. Higher amplitudes of V_P are obtained at the intermediate velocity u_2 where the repetition frequency of the vortices is near the resonant frequency f_m = 13.6 Hz of the beam. From the frequencies f_{u1}, f_{u2} and f_{u3}, of the main components in the signal spectra, the Strouhal number $St = f_u W/u \approx 0.17$ has been determined for the proposed configuration [3]. The ability of this harvesting system to power autonomous sensors has been demonstrated by connecting the converter to a tailored energy management and signal conditioning circuit plus two sensors [4], as shown in Fig 4. Once enough energy has been stored in the capacitor C_S a rectangular-wave voltage V_{TM} is generated which simultaneously carries information on both the flow temperature measured by a resistive sensor NTC Epcos K164/10k and the beam oscillations. The frequency of V_{TM} depends on the flow temperature and the duty cycle is modulated by the signal form a piezoelectric sensor placed on the cantilever to sense the deflections. The V_{TM} signal is transmitted by an RF OOK modulator (315 MHz). An external receiver unit can extract both the flow temperature and the velocity by the frequency of the forcing vortices, enclosed in the oscillation information, and the known *St* number. As shown in Fig. 5, harvested power up to 650 μW has been obtained. Correspondingly a retransmission interval below 2 min has been achieved. As it can be observed best performances are obtained for flow velocities, of about 4 m/s, that excite the beam resonance.

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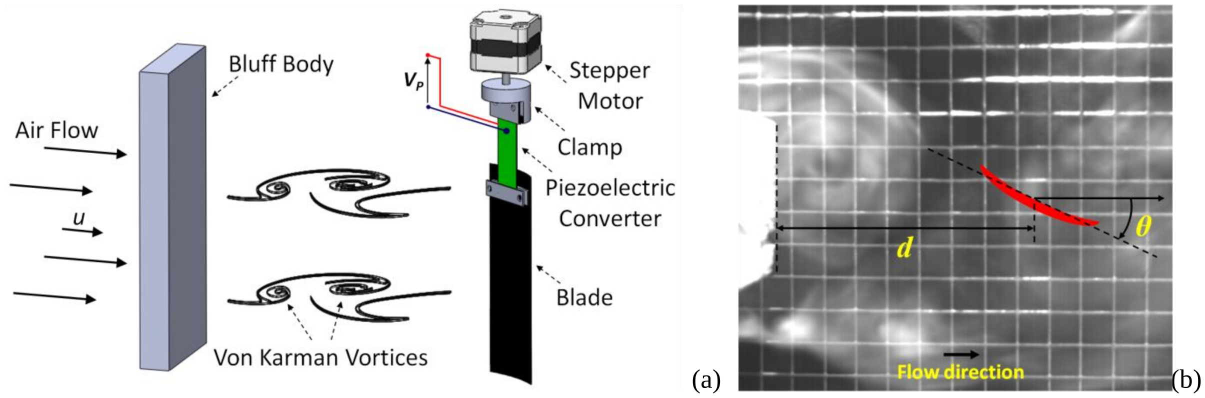

Figure 1: (a) Sketch of the system: the bluff body is W = 55 mm wide, the piezoelectric converter is 45 mm long and 20 mm wide and the blade is 70 mm long and 30 mm wide. The stepper motor allows to change the orientation angle of the beam with respect to the flow direction. (b) Visualization of the flow pattern by smoke: the position of the blade at d = 80 mm from the bluff body, and the orientation angle θ are shown.

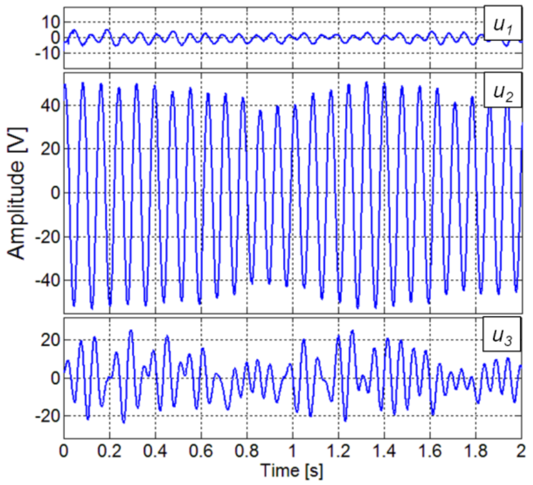

Figure 2: Voltage V_P versus time measured for three different flow velocities, u_1 = 2.3 m/s, u_2 = 4.2 m/s, and u_3 = 6.2 m/s for θ = 300°.

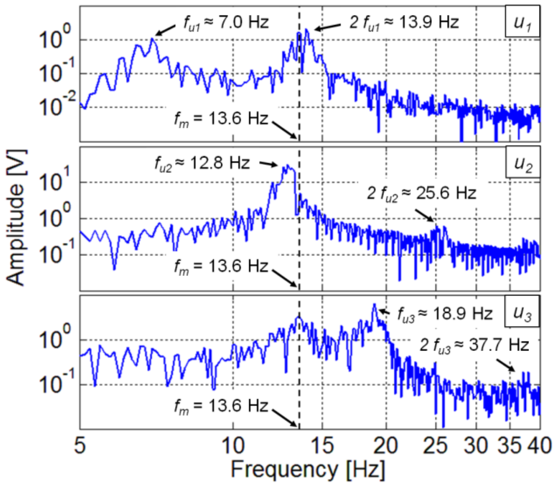

Figure 3: Frequency spectrum of V_P measured for three different flow velocities: u_1 = 2.3 m/s, u_2 = 4.2 m/s, and u_3 = 6.2 m/s for θ = 300°.

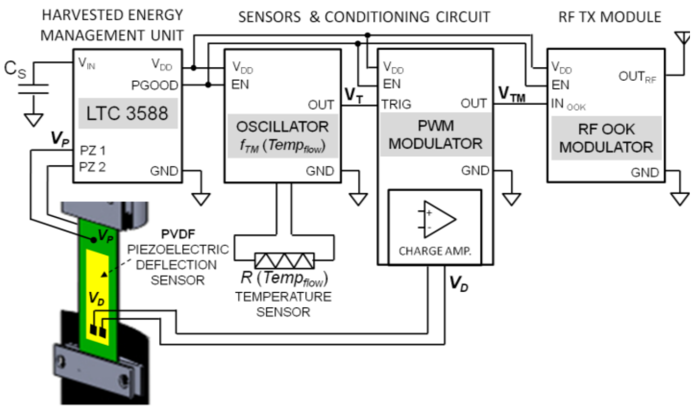

Figure 4: Block diagram of the autonomous sensor module powered by the piezoelectric converter. The voltage V_{TM} has frequency and duty-cycle sensitivities of 30.3 Hz/°C and 0.59 V^{-1} respectively.

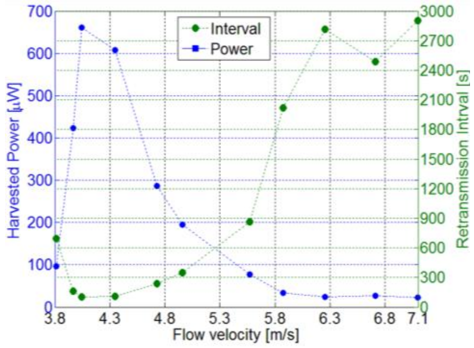

Figure 5: Average harvested power and retransmission time interval as a function of the flow velocity.

Contactless Interrogation of Quartz Crystal Microbalance Sensors by an Electronic Interface Using a Time-Gated Technique

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Understanding the different biological properties of samples demands investigations ranging from the tissue level all the way down to individual proteins and DNA, and consequently involves a huge range of different approaches and kind of sensors. Among these, quartz crystal microbalance (QCM) sensors are able to measure the changes in mass and viscoelastic properties close to the sensor surface across a range up to a few micrometers, and seem to be suitable for the characterization of microsamples in mechanobiology experiments. The studies of biological properties often demand for enclosed environments with constant temperature, therefore cabled solutions are generally impractical [1], while the possibility to exploit contactless interrogation techniques via electromagnetic coupling is attractive. Among the viable solutions, the time-gated technique exploiting the decaying response of the resonator is independent of the distance of interrogation, which only affects the signal amplitude [2].

This work proposes and experimentally validates a compact circuit solution based on Direct Digital Synthesis (DDS) for the contactless interrogation of QCM sensors that exploits heterodyne demodulation and autocorrelation analysis to measure the sensor response avoiding the use of expensive instruments. Fig.1 shows the block diagram of the developed contactless interrogation system. The interrogation unit employs the primary coil L_1 electromagnetically air-coupled to the secondary coil L_2 of the sensor unit connected to the electrodes of the QCM sensor. Programmable high frequency-resolution DDS devices (DDS1 and DDS2) generate the excitation and the gating signals. During the excitation phase, the QCM sensor is excited around its fundamental thickness resonant frequency by the electromagnetic coupling between L_1 and L_2, while during the detection phase, the excitation signal is disconnected and the resonator undergoes decaying oscillations at frequency f_{dm} forcing a current in L_2. Consequently, an induced readout voltage V_1 can be sensed across L_1 by the high-impedance readout circuit A_3. The analog multiplier M1 performs the heterodyne demodulation by mixing the sensor signal V_{01} with the reference signal V_r provided by DDS3, as shown in Fig. 2. The low-pass filtered beat signal V_{out} is then acquired by a low-cost ADC (12 bits, 25kS/s), and the resonant frequency and Q-factor of the resonator are derived by autocorrelation analysis. At present, this is done by a dedicated LabVIEW program on a PC, as shown in Fig. 3. Fig. 4 shows the estimated frequency and Q-factor values of a QCM sensor for different values of the interrogation distance *d*. As expected, the measured values are independent of *d*, and repeated measurements show standard deviations σ less than 1.6 Hz and 1500 for the frequency and Q-factor, respectively. Tab. 1 reports the series resonant frequency f_s and Q-factor reference values of three different QCM sensor taken with an impedance analyzer (HP4194A) and the estimated data given by the contactless interrogation system at four different *d*, showing an excellent agreement. The proposed technique measures both the series resonant frequency and the Q-factor of the QCM, allowing in principle to derive the viscoelastic behaviour of microsamples which is attractive for mechanobiology experiments.

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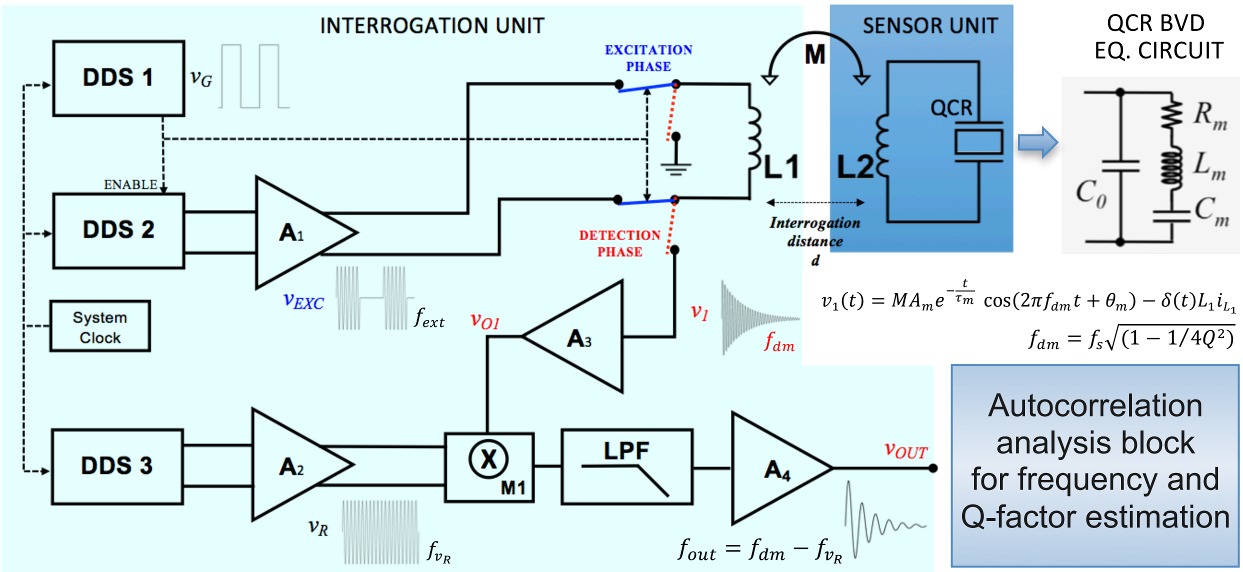

Figure 1: Block diagram of the DDS-based Interrogation Unit and Sensor Unit. L_1 and L_2 represent the primary and secondary coils, respectively. The analog multiplier M1 performs the heterodyne demodulation by mixing the sensor signal v_{O1} with a reference signal v_R provided by DDS3.

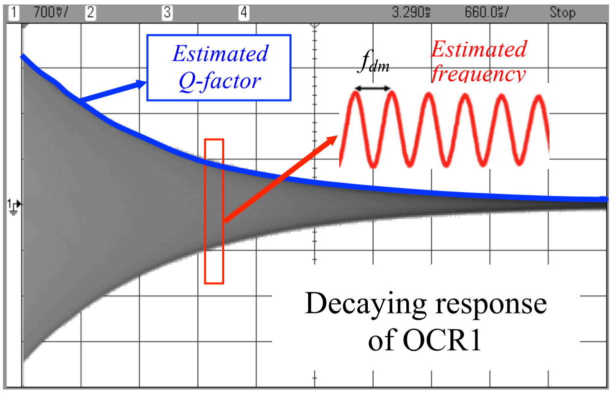

Figure 2: Typical signal v_{O1} representing the dacaying response of the contactless interrogated 4.8-MHz QCR1 sensor during the detection phase ($d = 5$ mm).

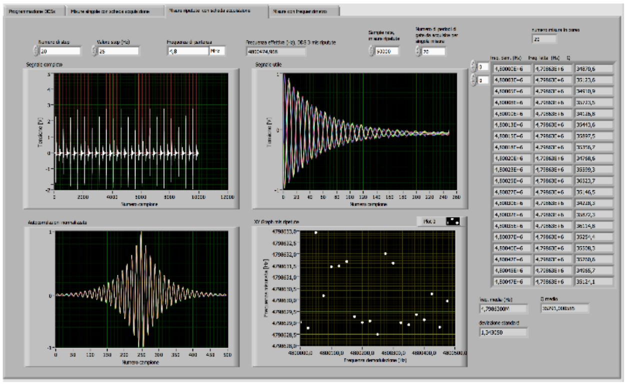

Figure 3: LabVIEW front panel with the acquired signals v_G and v_{OUT}, the autocorrelation analysis, and estimated values of frequency f_{dm} and Q-factor.

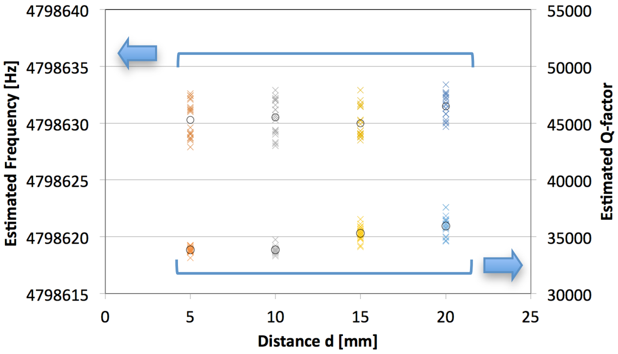

Figure 4: Estimated frequency f_{dm} and Q-factor values of QCR1 sensor from measurements taken at different values of the interrogation distance d.

Table 1: Reference and estimated values of frequency and Q-factor for three different QCR sensors.

QCR 1 – Ref. Meas.: fs = 4798948 Hz, Q-factor = 38720 (HP4194A)				
d [mm]	Est. frequency f_{dm} [Hz]	σ [Hz]	Est. Q-factor	σ
5	4798630.3	1.60	33833	248
10	4798630.5	1.57	33848	382
15	4798630.0	1.34	35291	586
20	4798631.5	1.07	35943	890

QCR 2 – Ref. Meas.: fs = 4431804 Hz, Q-factor = 31553 (HP4194A)				
d [mm]	Est. frequency f_{dm} [Hz]	σ [Hz]	Est. Q-factor	σ
5	4431470.0	0.92	29455	103
10	4431470.4	0.28	30604	129
15	4431470.2	0.82	31115	237
20	4431473.2	0.68		

QCR 3 – Ref. Meas.: fs = 3276344 Hz, Q-factor = 204470 (HP4194A)				
d [mm]	Est. frequency f_{dm} [Hz]	σ [Hz]	Est. Q-factor	σ
5	3276264.4	0.10	185137	1514
10	3276264.0	0.13	188093	1111
15	3276264.6	0.08		
20	3276264.6	0.04		

Influence of film microstructure on gas sensing in metal oxide nanograined chemosensors

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Abstract

In order to improve sensitivity, metal oxides sensors are based nowadays on nano-structured materials, i.e. a porous films with grain diameter that can't be considered large with respect to the Debye length.

It is known that when the grain dimension goes below a certain critical dimension the influence of the grain geometry becomes important and strongly influences the sensor response. In a previous work the case of nanowire was treated by the authors [1]. In this work the case of spherical grains will be discussed in order to point out that the reduction of the sensing film grain size significantly changes the behavior, not always giving a better performance in terms of sensitivity with respect to large grained films. The model was focused on p-type material and some simulation results for $YCoO_3$ are shown and discussed.

The model takes into account a spherical particle of homogeneous material, with radius R_g and a certain amount of charges localized at the surface due to the presence either of intrinsic ionizable defects and of chemisorbed molecules with a total surface density N_s. When the equilibrium is reached, an electric field is generated in the grain to counterbalance the diffusion of free carriers which are attracted or rejected from the bulk toward the surface. In a p-type semiconductor where the bulk hole density is p_b and the free electron density is negligible, the trapped charge causes the formation of a depleted negative charged layer below the surface extending to the inner of the grain and of an electric field that hinders the movement of holes from the inner to the surface. The negative charge density, ρ, in the grain at the thermal equilibrium can be found by balancing the diffusion current related to the charge density gradient and the hole drift current driven by the electric field. Considering an homogeneous grain and an uniform charge density at the surface all quantities expressed in spherical coordinates depend only by the distance from the sphere center r, so the charge density can be found from the following equations:

$$J_{tot}(r) = \sigma_p E(r) - qD_p \frac{\partial p(r)}{\partial r} = 0; \tag{1}$$

Where J is the current density, E the electric field, $\sigma_p = qp(r)\mu_p$ is the hole conductivity and μ_p is the hole mobility, D_p is the diffusion coefficient of holes and $Dp=\mu_p\, kT/q$, and $p(r)$ is the hole density. Starting from it we can obtain the following integral-differential equation:

$$\mu_p(qp_b - |\rho(r)|)\int_0^r |\rho(u)|u^2 du = \varepsilon D_p r^2 \frac{\partial|\rho(r)|}{\partial r} \tag{2}$$

Where $0 \le |\rho(r)| \le qp_b$ and $\rho(0)$ assume a value that grants the following electro-neutrality condition:

$$4\pi\int_0^{R_g} \rho(u)u^2 du = 4\pi R_g{}^2 qN_s\,. \tag{3}$$

These two equations can be solved numerically and some results are shown in Figures 1-2. For numerical evaluation the bulk density of holes is considered 10^{16} cm^{-3}, and the electrical parameters of $YCoO_3$ are taken from [2].

Note that if the grain is close to full depletion a decreasing of gas sensitivity is expected, because the sensing mechanism is close to the saturation. For a p-type oxide this can reduce sensitivity to reducing gases and a better performance with oxidizing gases are expected.

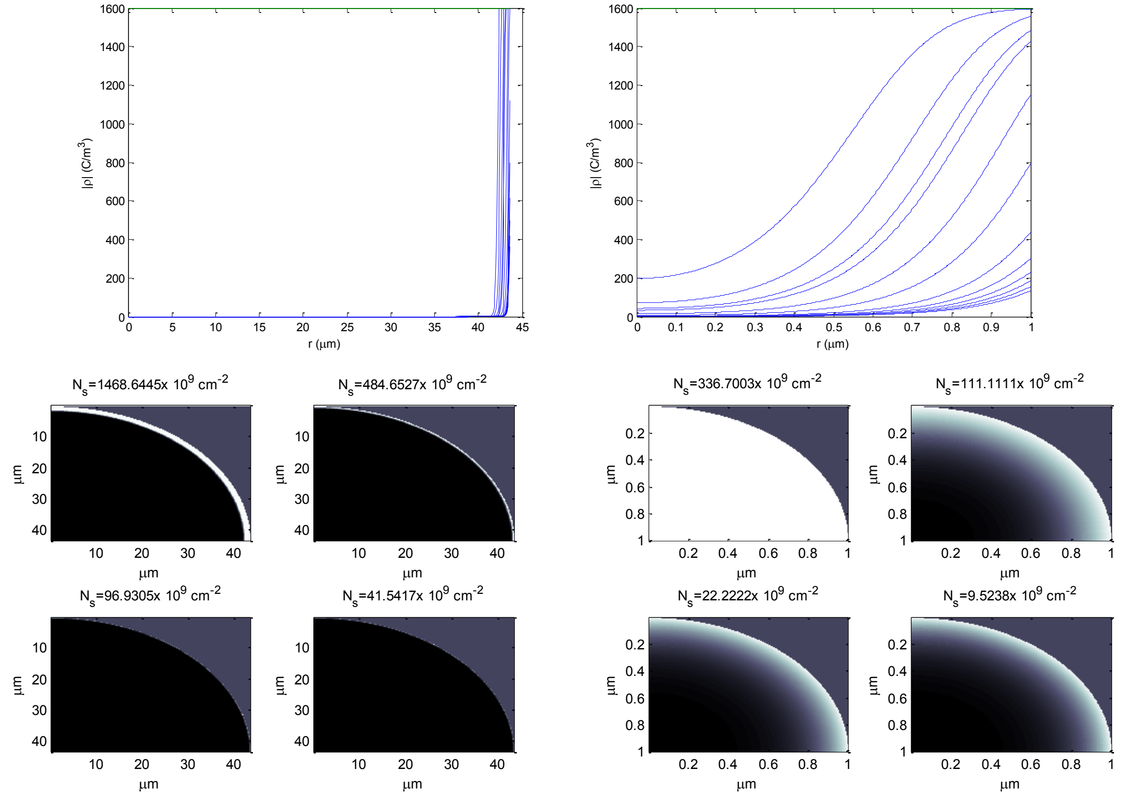

Figure 1. Charge density in the grain. Comparison of 'large grain' (R_g>>λ_D) (left) and 'small grain' behavior (right) for a material similar to those proposed in this work. In the lower plots the charge density is gray-level coded. The parameters for the numerical calculation are taken from [2]

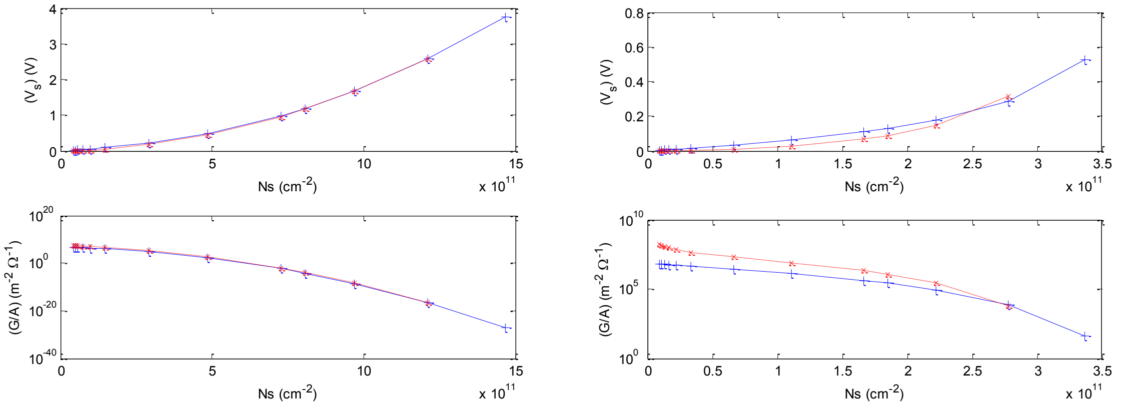

Figure 2. Comparison of 'large grain' (R_g>>λ_D) (left) and 'small grain' behavior (right) for a material similar to those proposed in this work. Higher plots: surface potential barrier; lower plots: normalized conductance

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Low-Noise Charge Preamplifier for Electrostatic Beam Position Monitoring Pick-Up at the ELENA Experiment

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The Extra Low ENergy Antiproton ring (ELENA) is a synchrotron under construction at CERN aimed to decelerate the antiprotons from the existing Antiproton Decelerator (AD) to an energy of 100 keV. The orbit measurement of the beam is accomplished by 20 electrostatic Beam Position Monitoring (BPM) sensors (pick-ups) to measure complete orbits every 20 ms with a resolution of 0.1 mm for intensities in the range of 1-3x10^7 charges. For the conditioning of the pick-up signals a low-noise charge amplifier has been purposely designed and is under testing.

The proposed design of the electrostatic pickups and the measurement principle is schematically represented in Fig.1. It comprises a stainless steel body containing two diagonal cut BPM pick-ups inserted into a vacuum tank, 100 mm diameter. The two pick-ups allow the measurement of the position in two orthogonal planes. The charged beam induces on the pick-up electrodes a charge which is measured by a pair of charge preamplifiers CA1 and CA2. The readout signals v_1 and v_2 from the preamplifiers are analogically combined to derive the sum (v_1+v_2) and difference (v_1-v_2) signals. The designed charge preamplifier circuit is shown in Fig. 2. The input stage is based on a NJFET/BJT folded cascode configuration. The two paralleled NJFETs J1 and J2 lower the noise voltage due to capacitance matching with the sensor, while the pnp BJT Q1 allows to down-shift the DC level with respect to a more traditional npn configuration [1-2]. The cascode pair is driven by an active load based on the npn BJT Q2 to obtain a voltage open-loop gain of about -6000. The emitter follower npn BJT Q3 decouples from the following stage and its output is capacitively fed back with a precision capacitance C_{FB}=1±0.05 pF to the JFET inputs. An additional feedback loop based on the AD811 current feedback amplifier with gain of 5 is adopted to implement a "cold" resistance mechanism to reduce the thermal noise of the feedback resistor R_{FB}=5 GΩ and to set the low corner frequency of the preamplifier at about 100 Hz [2]. Capacitance C_A=3 pF sets the high corner frequency to 40 MHz. Modeling the signal from the BMP pick-up with an equivalent voltage source v_S and considering the source capacitance C_S of about 26 pF inclusive of the cables and the pick-up electrodes, a voltage gain v_{out}/v_S of 42.3 dB can be estimated. Additional inputs CAL1 and CAL2 are used to calibrate the gain of each charge amplifiers. The estimated gain v_{out}/v_{cal} is about -14 dB. Fig. 3 shows a picture of the first prototype. Fig. 4 shows the simulation results of the output noise power spectral density of the preamplifier as well as the contribution to the noise due to the NJFETs and the feedback resistor. In the bandwidth 100 Hz-40 MHz a noise voltage density lower than 0.4 nV/$\sqrt{\text{Hz}}$ is obtained, that meets the challenging requirements. Fig. 5 reports the frequency response measured for the charge amplifier CA1 by using the calibration input CAL1 which shows good agreement with the simulation results both for the low and high corner frequencies of 99 Hz and 39.7 MHz respectively and for the midband gain of about -15.33 dB. After amplification, the sum and difference signals are analogically derived and sent over 50 m cables to further blocks for digitalization and processing.

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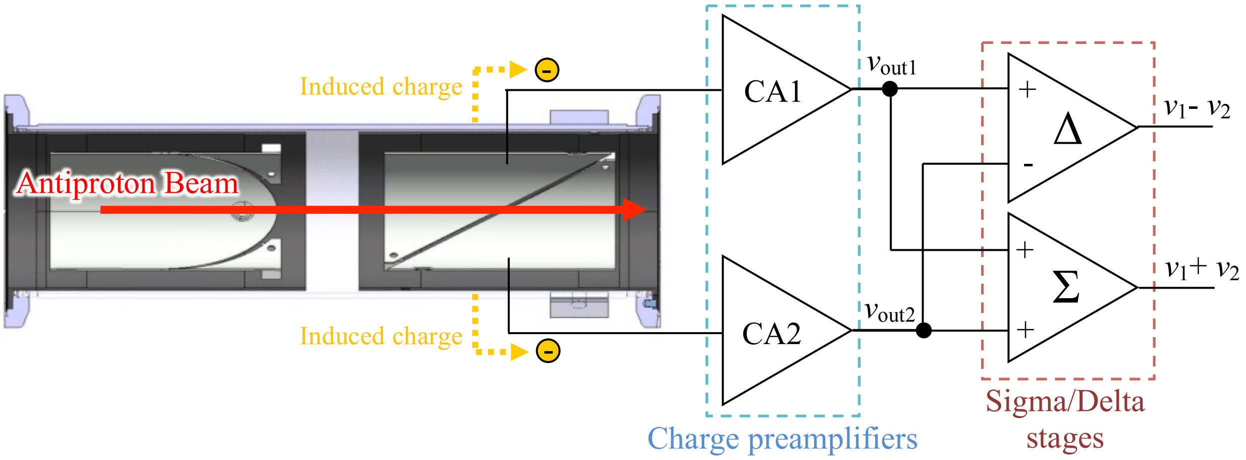

Figure 1: Cross section view of the ELENA BPM pick-ups with a view of the two diagonal-cut sensors and the measurement principle for each pick-up.

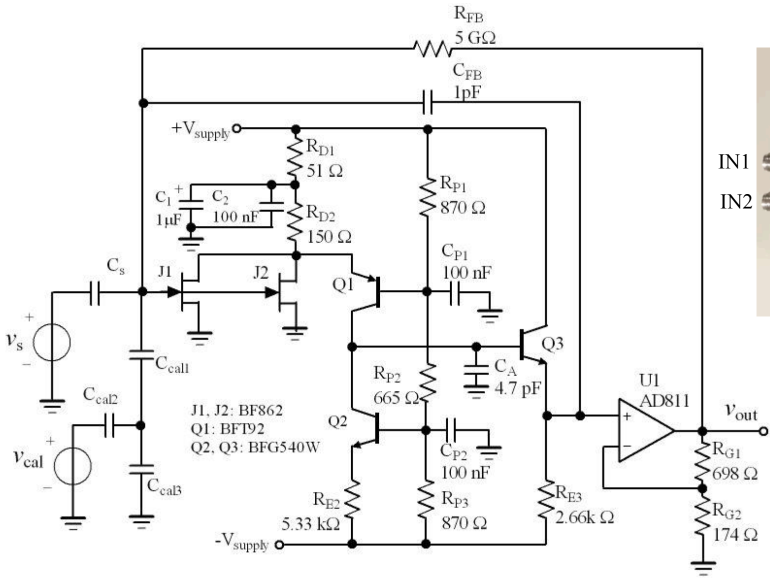

Figure 2: Circuit diagram of the charge preamplifier.

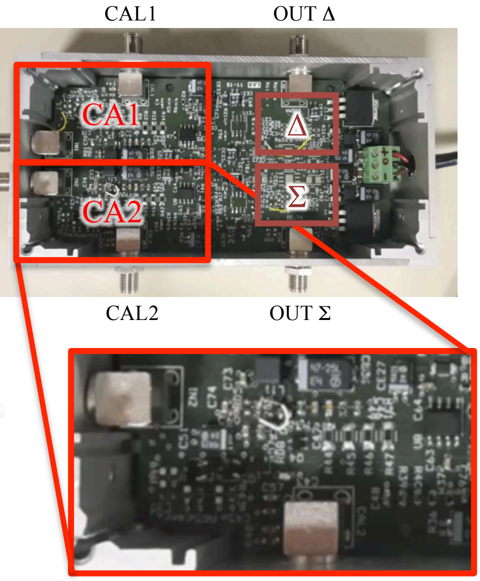

Figure 3: Picture of the prototype.

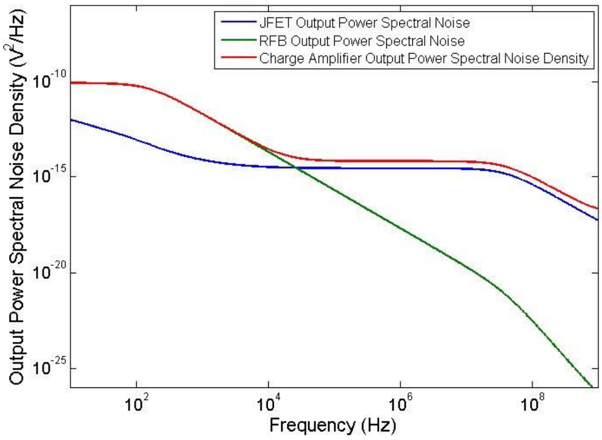

Figure 5: Simulation results of the output noise power spectral density of the charge amplifier.

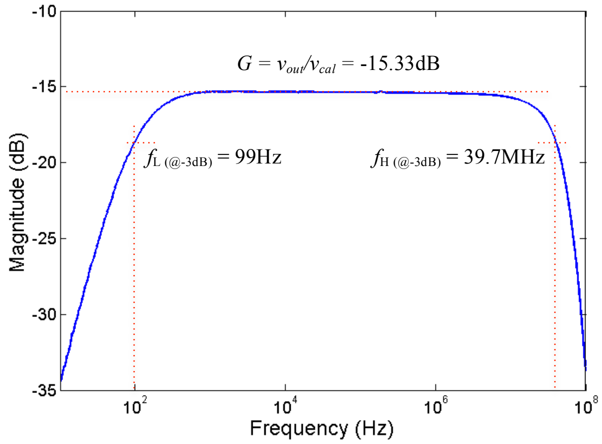

Figure 6: Frequency response measured for the charge preamplifier CA1 obtained by using calibration input CAL1.

MEMS electrostatic force actuator with capacitive position sensing

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Microactuators and microsensors are interesting tools to test mechanical properties of materials at the microscale [1] and are especially promising for probing biological samples in *in-vitro* mechanobiology experiments. As examples, flexible-beam optical and capacitive force sensors have been reported for cellular force measurement [2, 3]. Typically, these configurations require external equipment to apply either the force or displacement, while the complementary quantity is measured by the microsystem.

In this work we propose a Micro Electro-Mechanical System (MEMS) that performs electrostatic force actuation and capacitive position sensing on the same chip. By driving the actuator with a given voltage, a known force can be applied to a microsample under test by using a silicon probe tip, while the obtained displacement is measured. This allows to extract the mechanical properties of the microsample entirely on chip, and to derive its force-displacement curve without external equipment. The description of the device, a proposed electro-mechanical model and experimental characterization results are presented. Figs. 1 and 2 show the operating principle with equivalent models and SEM images of the device, respectively. The probe tip shown in Fig. 2c can be used to press the microsample, represented by its mechanical impedance Z_L, by applying a known force, which can be set by imposing a proper driving voltage V_{DR} to the variable-area comb driver capacitor, while the variable-gap comb sensing capacitor C_{SR} is used to measure the probe tip displacement x. To calibrate the applied force as a function of the voltage V_{DR}, a calibration procedure by using the weight force as reference has been adopted. A tilting of the device to +90 and -90 deg around the y axis has been imposed while keeping the displacement x unaltered by feedback adjustment of V_{DR}. In this way, the mechanical stiffness k_m of the spring has no effect on the calibration. Fig. 3 shows in the inset how the mass m_m has been estimated as 21.6 μg from the theoretical value of the electro-mechanical transduction factor $\alpha_{DR} = F_{DR}/V_{DR}^2$, and plots the experimental values of α_{DR} at varying voltage V_{DR} thereof obtained in the calibration procedure. Fig. 4 shows the blocked (zero displacement) force F_{DR} provided by the electrostatic actuator as a function of voltage V_{DR}, while Fig. 5 shows the measured capacitance C_{SR} as a function of displacement x. The displacement x has been calculated taking into account the parasitic capacitances, which have been estimated as in [4]. Hence, by using the calibration curves of Figs. 4 and 5, the microsample force-displacement behavior can be obtained without external equipment. Fig. 6 shows the force-displacement characteristic of the device measured in free condition by varying the applied voltage V_{DR}. In such a case, only the stiffness $k_{\mathrm{m}} = 3.44$ N/m of the spring of the device was measured, since no microsamples were actuated by the probe tip. The proposed device allows to measure in both static and dynamic regimes, therefore it could derive the complete viscoelastic behavior of the microsample in mechanobiology experiments.

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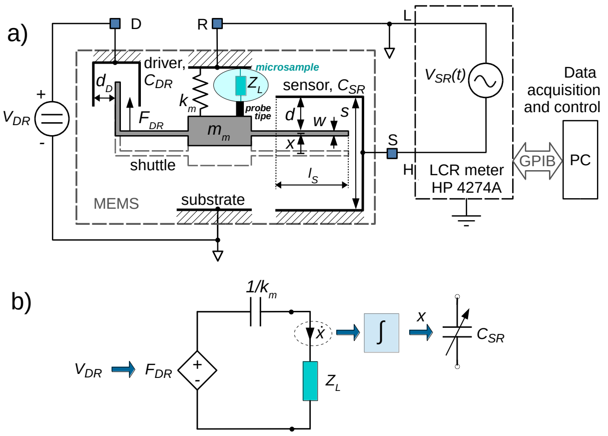

Figure 1: Monodimensional equivalent mechanical model of the device with the electrical setup (a) and equivalent electro-mechanical lumped-element circuit (b).

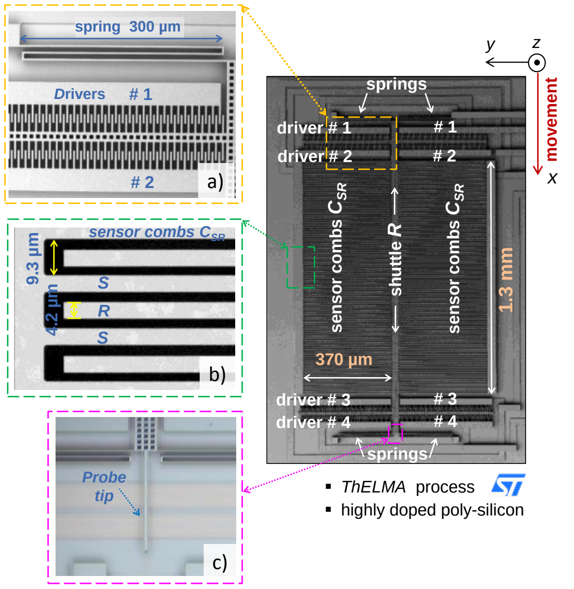

Figure 2: SEM images of the device with enlarged views of drivers and spring (a), a set of parallel plate of the displacement sensor(b) and the probe tip (c).

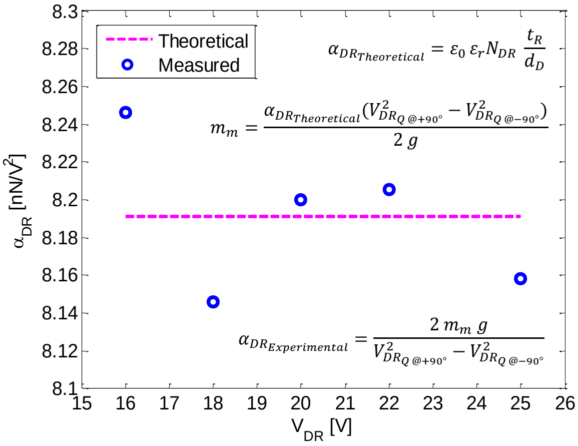

Figure 3: Theoretical and measured electro-mechanical transduction factor α_{DR} as a function of the applied voltage V_{DR}.

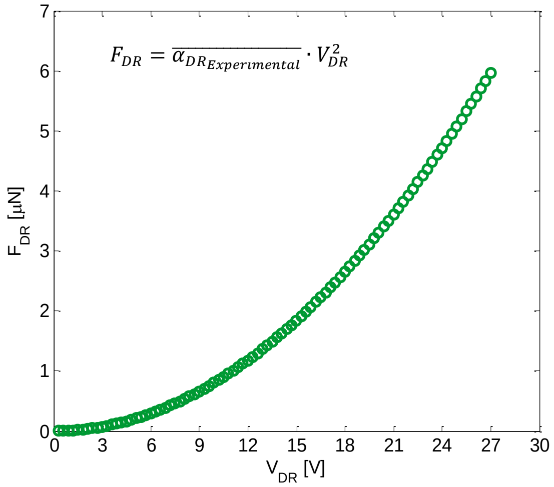

Figure 4: Blocked (zero displacement) force F_{DR} provided by the electrostatic actuator as a function of the applied voltage V_{DR}.

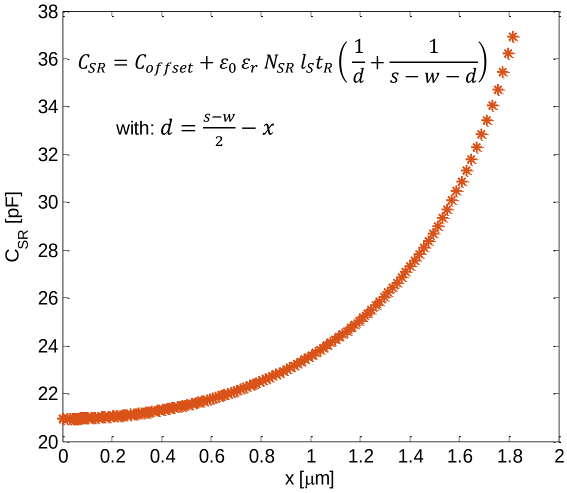

Figure 5: Measured capacitance C_{SR} as a function of displacement x obtained with the electrical setup shown in Fig 1b.

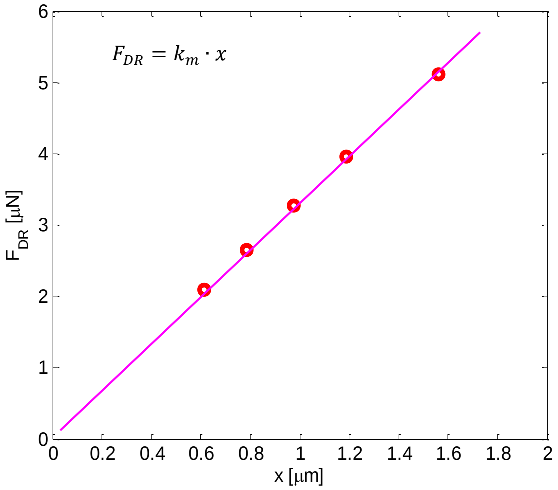

Figure 6: Experimental force-displacement characteristic of the device in free condition (zero load). The mechanical stiffness k_m of the spring results 3.44 N/m.

NanoSQUID Sensors to Investigate Magnetic Properties of Nanoparticles

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In the recent years, it has been shown that the magnetic response of nano-objects (nanoparticles, nanobead, small cluster of molecules) can be effectively measured by using a Superconducting Quantum Interference Device (SQUID) with a small sensitive area. In fact the sensor noise expressed in term of the elementary magnetic moment (Bohr magneton, μB) is linearly dependent on the SQUID loop side length. For this reason, LTc SQUIDs have been progressively miniaturized in order to improve the sensitivity up to few tens of μB per unit of bandwidth.

The nanosensor consists of a niobium loop interrupted by two Dayem nanobridges as shown in Fig.1. We have designed and fabricated nanoSQUIDs consisting in a square hole with an inner side length of 0.75, a width of 0.2 and two Dayem bridges 120 nm long and 80 nm wide. Two different configurations have been used: one where the bias leads are symmetric with respect to the loop and the other one with a strong bias asymmetry which corresponds to an inductance loop asymmetry. As we will show in the experimental results, the last configuration allows us to improve the critical current responsivity. The characterization of the nanodevice in the temperature range from 1.2K to 4.2 K includes measurements of current-voltage, critical current vs. magnetic flux characteristic[1,2,3,4]. A proper feedback circuit has been employed to increase the dynamic range of the nanosensor and to measure the M(H) curve of magnetic nanoparticle, whereas the sensors are employed in the small signal mode regime for the magnetic relaxation measurements[2].

The magnetic nanoparticles under investigation have a diameter of 4 nm and 8 nm. Measurements of magnetization as a function of the external magnetic field for both nanoparticle diameters are reported at liquid helium temperature. In both case it can be observed an evident magnetic histeresis indicating a blocking temperature well above 4.2 K. Magnetic relaxation measurements with a time resolution below 0.1s have also been performed and will be shown. The measurement in higher magnetic fields (up to 8 Tesla) and at lower temperature (down to 10mK) are under development.

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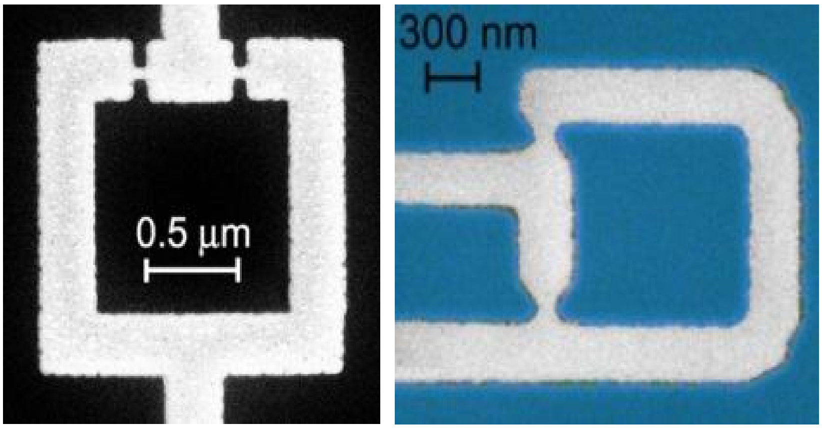
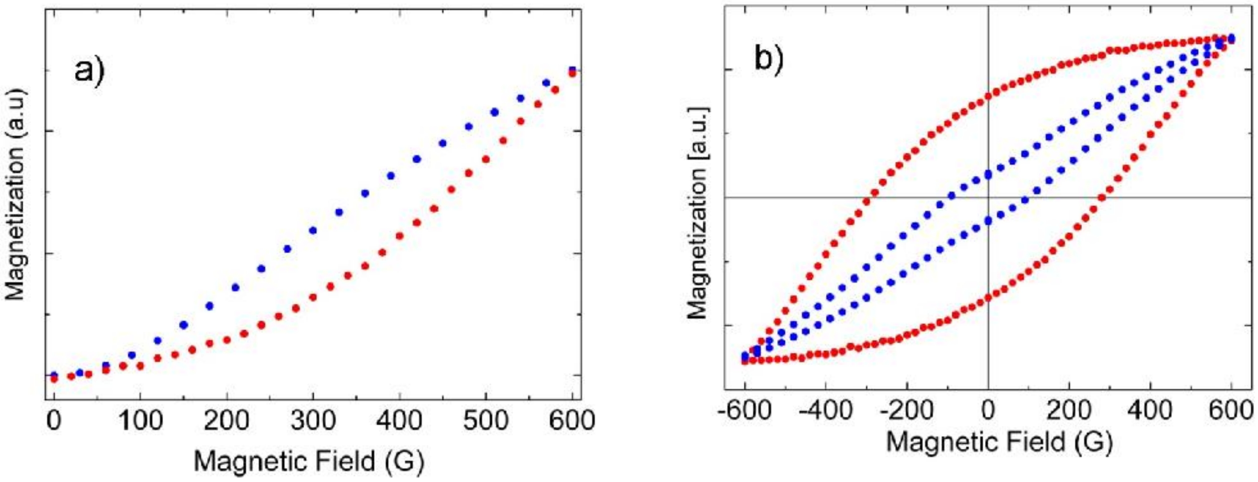

0.5 µm
300 nm


a)
Magnetization (a.u)
Magnetic Field (G)
0
100
200
300
400
500
600
b)
Magnetization [a.u.]
Magnetic Field (G)
-600
-400
-200
0
200
400
600

O_2 and CO_2 Voltammetric Sensors using Liquid Interaction

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Continuous monitoring of Oxygen and Carbon dioxide concentration is crucial for many different application fields, ranging from bio-medical studies to food-packaging processes and environmental monitoring. This is due to the role of these gases in important biochemical reactions [1] and more in general in the air quality determination [2]. Different application fields require different concentration ranges, but on-field and on-line applicability is of course mandatory. The state of the art is represented by electrochemical, optical and conductometric approaches [3-4], with excellent pros and not negligible cons.

Here a system for O_2 and CO_2 measurement is proposed. The system is composed of two parts: a voltammetric sensor [5] and a liquid interface in which the selected gas are conveyed for the volatmmetric analysis. The voltammetric sensor used in this work consists of a probe (commercial screen printed electrodes) and a dedicated electronic interface. The measuring probe is composed of three electrodes: 1) the working electrode (gold); 2) the counter electrode (Platinum); 3) the reference electrode (Silver). A dedicated software interface controls all the input and output parameters. The input signal is a triangular waveform between -1 V and +1 V, at a frequency of 0.01 Hz. The output signal is acquired with a sampling time of 1s thus collecting 100 samples of output current, treated as a single 'fingerprint' composed of a virtual array of 100 sensors. This system has been calibrated to Oxygen (5%, 10%, 15%, 20%, 25%, 30%, 35%, 40%, 50% with N_2 as carrier gas) and Carbon Dioxide (2%, 3%, 4%, 5%, 10%, 15%, 20% with N_2 as carrier gas) concentrations, using the experimental setup reported in figure 1.

The data set has been analyzed via multivariate techniques. A PLS-DA model was built in order to show sensor ability in the detection of O_2 and CO_2 detection at the concentration levels of interest. In figure 2 and figure 3 the plots of measured vs predicted concentration for O_2 and CO2 respectively are reported. The Root Mean Square Errors in Cross validation are around 2% for both O_2 and CO2, which is promising both for IAQ (Indoor Air Quality) and breath analysis applications.

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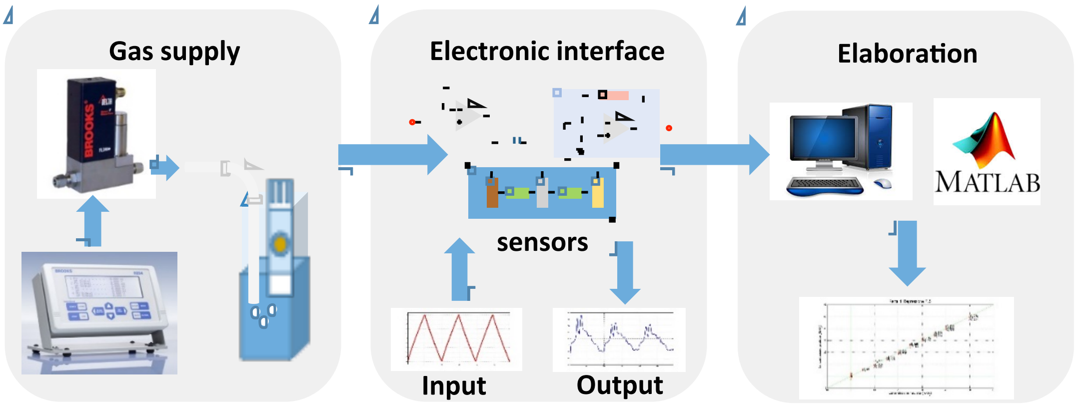

Figure 1: Experimental setup

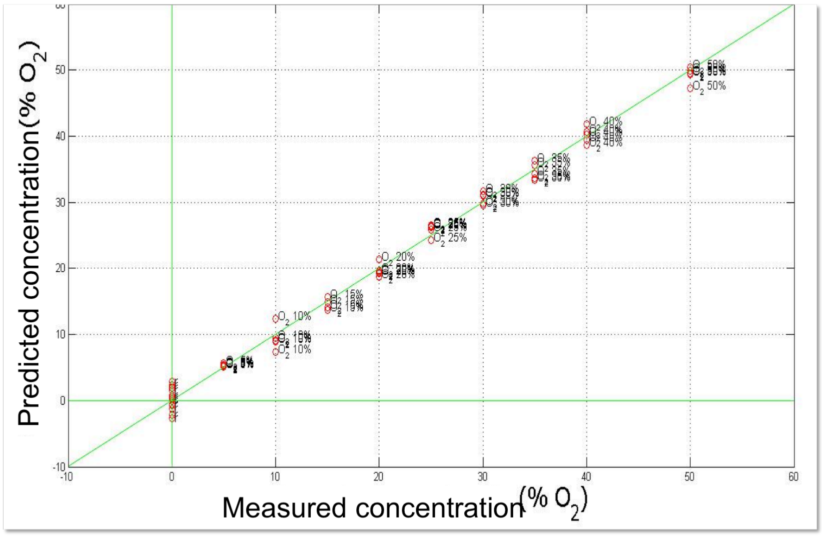

Figure 2: PLS-DA plot of O_2 % predicted vs measured

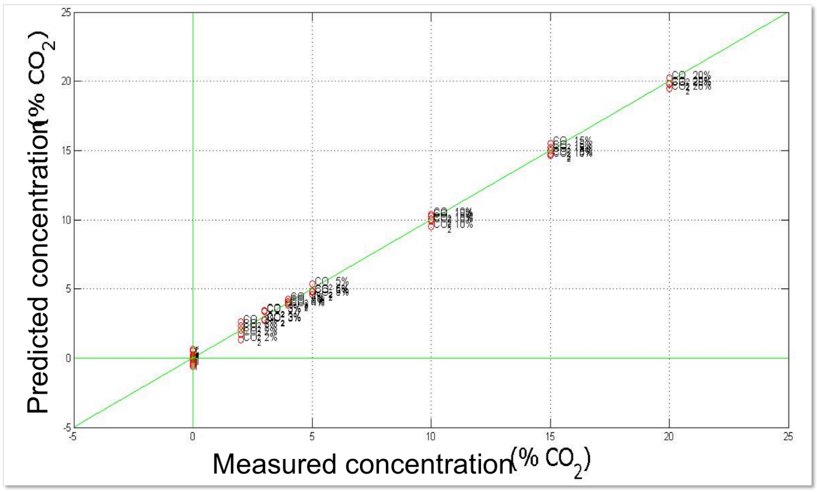

Figure 2: PLS-DA plot of CO_2 % predicted vs measured

On-Body Battery-Less Sensor Powered by Ball-Impact Piezoelectric Converter

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Nowadays, due to the development of low-power devices and wearable electronics, on-body sensor systems powered by energy harvesting techniques are of great interest [1-2]. In this context, an on-body battery-less temperature sensor system powered by mechanical energy harvested from human motion through the piezoelectric effect is presented.

The developed autonomous sensor system is composed of a triaxial ball-impact piezoelectric converter, a tailored power management circuit, and a wireless temperature sensor module. The piezoelectric converter is composed of six piezoelectric diaphragms which surround a steel ball in a cube-shaped geometry providing multi-degree-of-freedom conversion (Fig. 1a). When mechanical excitations are provided, the driving ball repeatedly bounces and hits one or more diaphragms (Fig. 1b) and consequently electric power is generated by the piezoelectric effect. The converter exploits both the multi-element and the impact techniques, which are particularly suitable to increase the effectiveness of the converter towards low-frequency random vibrations and rotations such as those provided by human motion (Fig. 1b). The piezoelectric converter was strapped on the ankle of a person (Fig. 1c) and experimentally characterized during walking and running activities (Fig. 2). While the person is running at 7 km/h, a peak instantaneous power of up to 16 mW is provided by each of the six piezoelectric diaphragms [3], while the average power is two orders of magnitude lower. The harvested power is typically too low and/or discontinuous to guarantee a continuous operation of low-power autonomous sensors. Thus, a power management circuit able to toggle between energy storage and delivery phases by using a custom CMOS trigger circuit was designed and realized [4]. The piezoelectric voltage v_{gn} ($n = 1\ldots\ 6$) are rectified by diode-based voltage doublers which are parallel-like combined to charge a single storage capacitor C_S. A step-up DC-DC converter (Texas Instruments TPS61221) exploits the energy stored into C_S to power the sensor module with a regulated 3.3-V supply voltage (Fig. 3). The wireless temperature sensor module is composed of a linear regulator (Texas Instruments TPS780300250), an 8-bit microcontroller (Microchip PIC12LF1840) with an internal analog temperature sensor and 10-bit ADC, and a 433-MHz transmitter (FS1000A), as shown in Fig. 4. The microcontroller performs eight consecutive acquisitions of the temperature and sends the average value through the UART output at 9600 bps, by On-Off Keying (OOK) modulation of the transmitter carrier. The wearable autonomous sensor was tied to the ankle of a person and tested during walking and running activities. After about 260 seconds of walking at 2 km/h, an energy of 1.4 mJ is stored in $C_S = 1$ mF and used to perform a temperature measurement and transmission of the data to a host PC through the wireless link (Fig. 5 and Fig. 6).

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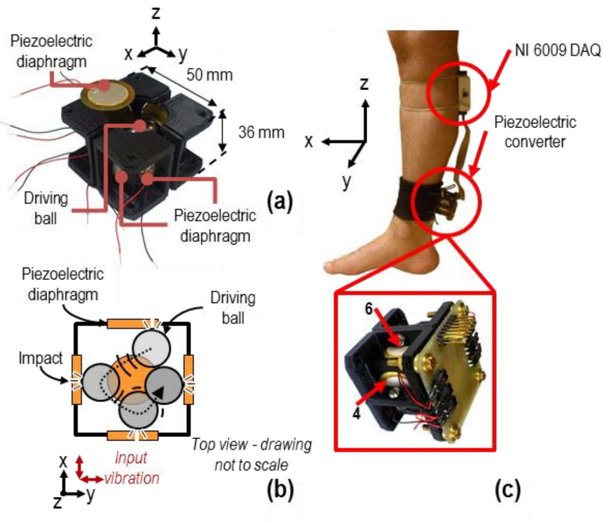

Figure 1: Fabricated prototype (a), schematic top view (b) and positioning of the converter strapped on the ankle of a person (c).

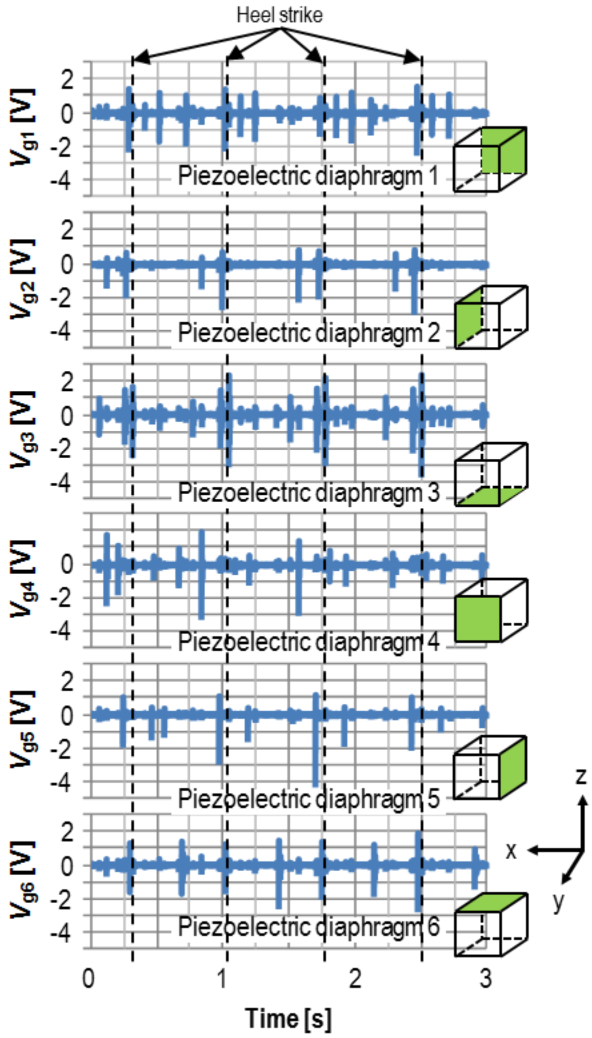

Figure 2: Voltages v_{gn} (n = 1… 6) provided on a 1-kΩ resistor by the piezoelectric diaphragms measured during a running session on the treadmill at 7 km/h.

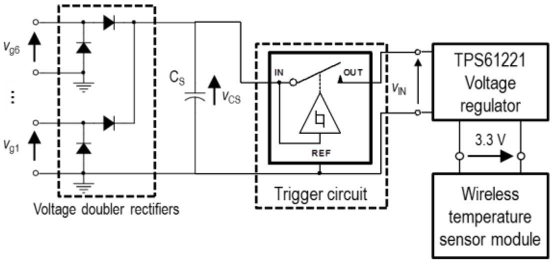

Figure 3: Block diagram of the power management circuit. When v_{CS} reaches V_{TH}, the trigger circuit toggles in the closed state and the voltage regulator powers the sensor module (energy delivery phase). When v_{CS} decreases to V_{TL}, the trigger circuit toggles in the open state, the voltage regulator and the sensor module are turned off, and a new charging cycle of C_S begins (energy storage phase).

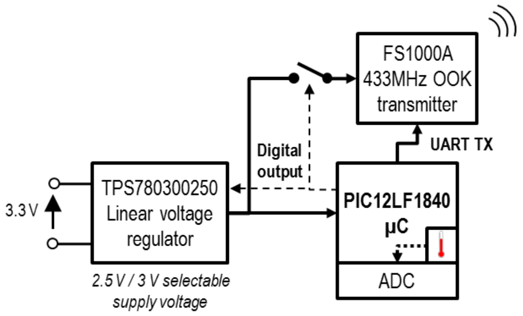

Figure 4: Block diagram of the proposed wireless temperature sensor module.

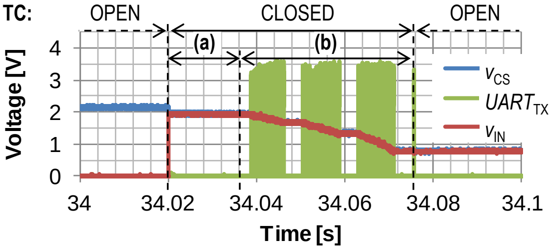

Figure 5: Experimental results of the autonomous sensor with the piezoelectric converted tied to the ankle of a person walking at 4 km/h. The data packet is sent three times, with random delays between retransmissions, in order to improve the robustness against noise and possible collisions.

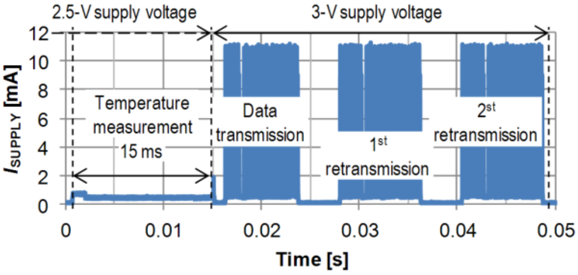

Figure 6: Measured supply current I_{SUPPLY} for the wearable sensor module during a measurement-and-transmission cycle.

Optoelectronic Sensors for Self Assembling Monolayer Detection

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Self Assembling Monolayers (SAM) autonomously form uniform layers over flat or nanostructured surfaces; they are widely used in biosensors, as they change the sensor surface properties and permit the binding of biological materials, spanning from whole cells down to short DNA fragments or proteins. SAMs are usually composed by methylene chains, bonding to the surface through the tail group (e.g., thiol on metals), while the head group determines the SAM surface properties.

Different electrical and optical techniques are used to sense the biosensor surface conditions. Among them, Surface Plasmon Resonance (SPR) is a powerful tool to sense analytes, such as chemicals, gasses, proteins, DNA and bacteria. SPRs occur when Surface Plasmon Polaritons (SPP) are excited. Moreover SPPs are evanescent electromagnetic wave propagating along a metal/dielectric interface [1].

In this paper we take advantage of the SPP coupling momentum sensitivity to interface variations to study the SAM growth kinetics on a silver grating surface, by measuring the azimuthal angle position ϕ of the SPR as a function of the time. By fully exploiting the SPR behaviour as a function of ϕ we introduce a new parameter for sensing the refractive index variation, i.e., the azimuthal sensitivity, defined as $\Delta\phi/\Delta n$. This parameter can reach values as high as 2180 deg/RIU if θ is carefully set [2] (see fig. 1). For comparison, with the Prism Coupling (PCSPR) configuration it cannot exceed the value of 200 deg/RIU [1] meanwhile with the Grating Coupling (GCSPR) configuration it can be enhanced up to 1000 deg/RIU [3].

To perform this experiment we excited the SPP by using a grating with 740 nm period and 20 nm amplitude, with a 50 nm Ag film sputtered on polycarbonate substrate mounted in conical configuration (see fig. 1). SAM was formed by flowing a solution of 6-mercapto-1-hexanol (MCH)/water 10 mM over the grating surface through a microfluidic cell.

Typical reflectance curves as a function of ϕ (fixed θ), are reported in fig. 2.a. In fig. 2.b the azimuthal position of the reflectance minima as a function of the time are reported. After the introduction of the MCH solution (t=20 min) the azimuthal peak position drops, since the MCH molecules quickly form a SAM on the silver surface. In fig 2.c we report $\Delta\phi = \phi_{MCH\,(t=50\ min)} - \phi_{Bare\,(t=5\ min)}$ as a function of ϕ_{Bare}. Experimental points are well fitted by an analytical model. The calculated sensitivity goes from a minimum of 390 deg/RIU up to 2700 deg/RIU.

By properly tuning and further enhancing such azimuthal sensitivity, this method could lead to a new class of SPR sensors with lower detection limits than actual ones.

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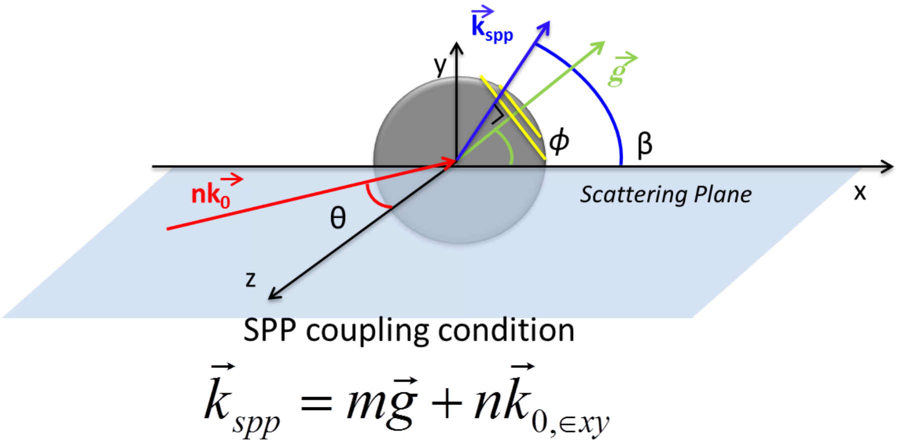

$$\vec{k}_{spp} = m\vec{g} + n\vec{k}_{0,\in xy}$$

Figure 1: Coupling condition for SPP: $\vec{k}_{spp}$ is the SPP momentum, $\vec{g}$ is the grating momentum (perpendicular to the grating slits), $n\vec{k}_0$ is the incoming light momentum, $m \in \mathbb{Z}$ represents the grating diffraction order that allows the SPP coupling, and n is the dielectric refractive index. θ is the angle between the incoming light and vector normal to the grating plane; ϕ is the angle between the grating momentum and the scattering plane.

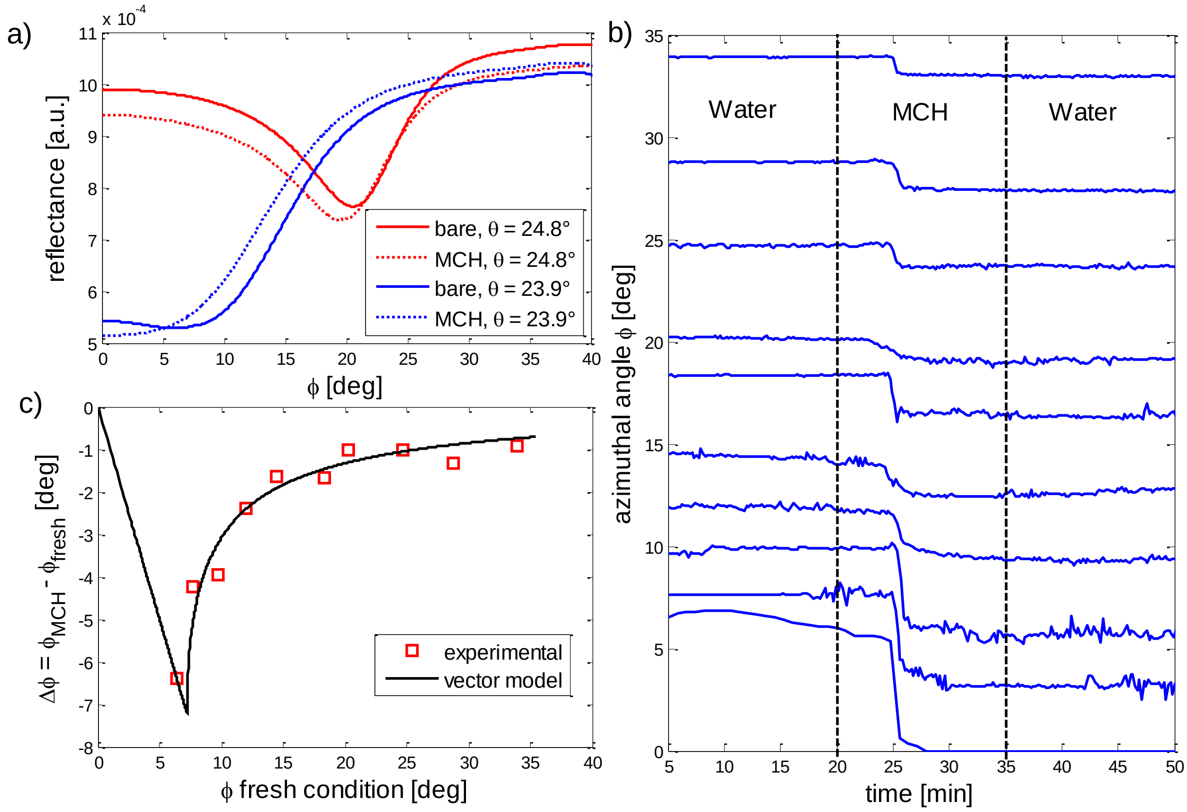

Figure 2: (a) Reflectance curves as a function of ϕ for the bare and MCH conditions measured at two different incident angles. Solid lines represent curves registered in the bare condition while dashed curves refers to the MCH condition. For θ = 24.8°, red curves, the azimuthal minimum appears at ϕ=20.6° and the MCH SAM causes a shift of this minimum to 19.5°. Setting θ = 23.9°, blue curves, the bare reflectance minimum appears at 6.2° and the MCH produces a single minimum at ϕ=0°.(b) Azimuthal peak as a function of the time; between 20 min and 35 min the solution were changed from water to MCH/water 10 mM and this causes a drop of the azimuthal peak position due to the SAM formation. (c) Azimuthal angle variations Δϕ as a function of the initial peak condition ϕ_{bare}

Photo-assisted chemical sensors based on porphyrins coated nanostructured ZnO

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Hybrid materials formed by a layer of dye molecules over a wide-band gap semiconductor, are widely studied mainly for optoelectronics and photovoltaic applications. However, besides the conversion of visible photons into an excess of carriers, the combination of organic-inorganic materials offers other additional properties such as chemical sensing. ZnO and porphyrins are a good example of the combination of a metal oxide semiconductor and a dye molecule. We have been interested to study the interplay of light and gas sensitivity in porphyrins-ZnO materials. For the scope we investigated ZnO nanorods prepared by hydrothermal route (fig. 1).

We shown that the conductivity of the hybrid material is both sensitive to the visible light and to donor-acceptor gases such as amines and alcohols [1]. Furthermore, under visible light the sensitivity increases and, most interestingly, the selectivity towards electron donor species (e.g. amines) is enhanced (see Fig. 2). It is important to note that the increase of selectivity is in general expected for Lewis basis. However, the case of amines is interesting because amines are relevant for food freshness and also for security issues being components of explosives and narcotics. The sensing properties of porphyrins coated ZnO have been further studied through the surface photovoltage. Kelvin probe signals demonstrate the interplay between the photosensitivity and the gas sensitivity suggesting that the adsorption of some volatile compounds may improve the photovoltaic properties of the dye-semiconductor hybrid (see fig. 3) [2].

The enhanced catalytic properties of porphyrins coated ZnO were studied in the past as electrochemical sensors for the detection of compounds in solution. Recenty we found that the exposure to visible light enhances both the sensitivity and the selectivity with respect to the detection of L-cysteine in water where the porphyrin coated ZnO is used as the work electrode of a voltammetric setup [3].

The sensing properties of layers of porphyrins onto ZnO nanostructures offer a further degree of freedom for the design of sensor arrays extending the properties and the capabilities of porphyrins based sensor array in particular for medical diagnosis, the quality and control of foods and the detection of compounds signalling harmful or dangerous substances.

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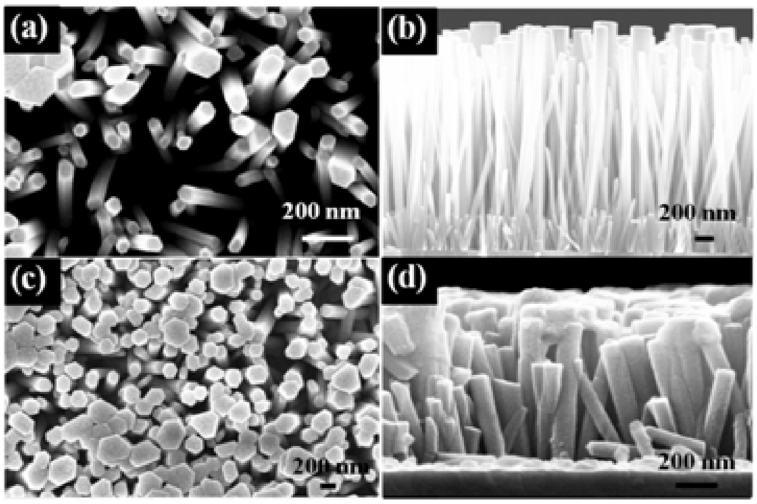

Fig. 2: FESEM images of nanostructures top and cross sectional view: (a) and (b) ZnO nanorods; (c) and (d) ZnO/Mn(Cl)TPPS; (e) and (f) ZnO/CuTPP

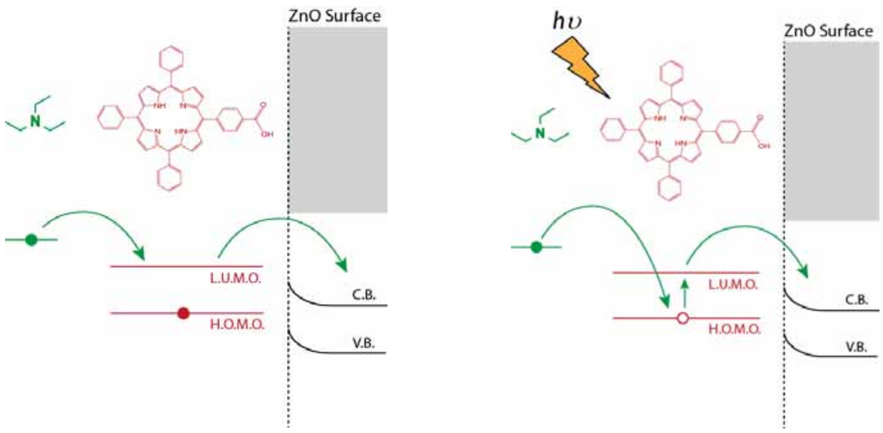

Fig. 1: the *charge transfer from a donor absorbed molecule in dark (left) is enhanced in light (b). In this last case, the light activates a charge transfer from the porphyrin to the ZnO. The depletion of electrons favours the charge transfer from the donor absorbed species.*

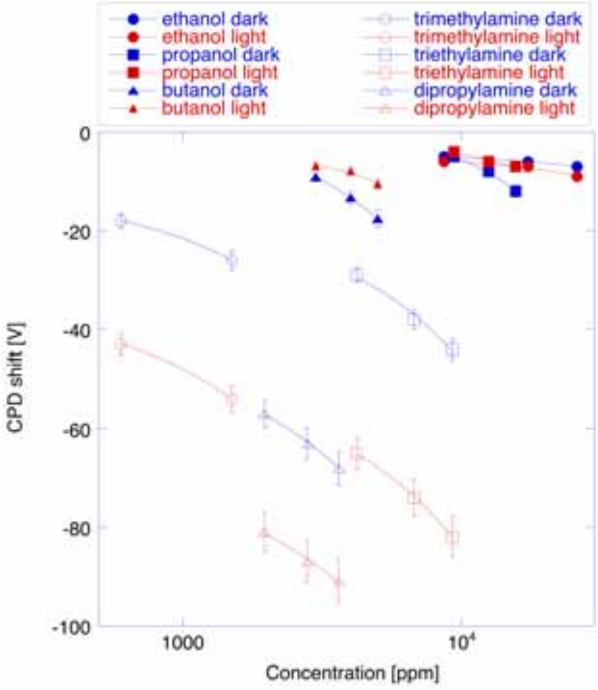

Fig. 3 contact potential difference shift, measured with a Kelvin probe, as a function of concentration for various amines and alcohols. The result evidences the improvement of sensor response prompted by the illumination with visible light.

Real Time PCR platform based on SiPM technology

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Biosensors importance, nowadays, is enhancing exponentially as well as their applications. The optical transduction mechanism is the most used method to recognize DNA hybridization with traditional markers in commercial devices (DNA chip and Real Time PCR). DNA microarray is based on the use of a probe (ssDNA) anchored on a surface, conjugated to a target molecule labelled with a fluorophore (e.g. CY5). An optical scanner is the detector [1]. In Real Time Polymerase Chain Reaction (RT-PCR) the fluorescence of Fluorescein (FAM) increases during the DNA amplification. In both systems an image analyser software is used, after acquisition, to quantify the signal and to allow a post-acquisition analysis.

Goal of our work is to replace the traditional detection systems, in both RT-PCR and DNA microarray applications, with a sensor based on a pixel array of solid state photon-detectors (Silicon Photomultipliers, SiPM), produced by STMicroelectronics in Catania. Each detector is an avalanche diode operating in Geiger mode and then they are connected in parallel to a single output [2]. Moreover, recent works describe the possibility to use SiPM as optical detector in biosensor applications [3]. In this work, SiPM formed by 25 pixels was used to detect the fluorescence of biological molecules.

To measure the fluorescence signal we used two similar experimental setup for DNA microarray [3] and RT PCR application (Fig. 1).

For example, the experimental setup used for RT PCR is described: a fibre-coupled laser hits orthogonally on the sample (~12µl in volume); the sensor is placed at 45° with respect to the normal axis to the sample inside a metal box, isolating optically and electrically the sensor from the external environment. Between the sensor and the sample is interposed a bandpass filter, centred at the fluorophore emission wavelength, in order to eliminate the contribution of the excitation laser radiation reflected by the support. The sensor is powered by a 236 Keithley SourceMeter, and the signal is acquired automatically using a software developed in Labview©, and, then, processed with Matlab©.

In order to determine the sensor detection limit FAM measurements in liquid (12µl) and CY5 spotted on solid surfaces, both at molar concentrations ranging from 500 fM to 5nM, were performed. We measured the fluorescence signal for different fluorophores concentrations and found that, for a fixed angle of analysis, the signal is linear over the measured range: 500fM - 5 nM (Fig. 2). This result underlines the higher sensitivity of SiPM than commercial optical system and so its ability to detect very low levels of fluorescence signal. The properties of SiPM and the set-up potentialities would allow one to miniaturise the system, opening up the possibility for the design and fabrication of a cheap, easy and portable optical system.

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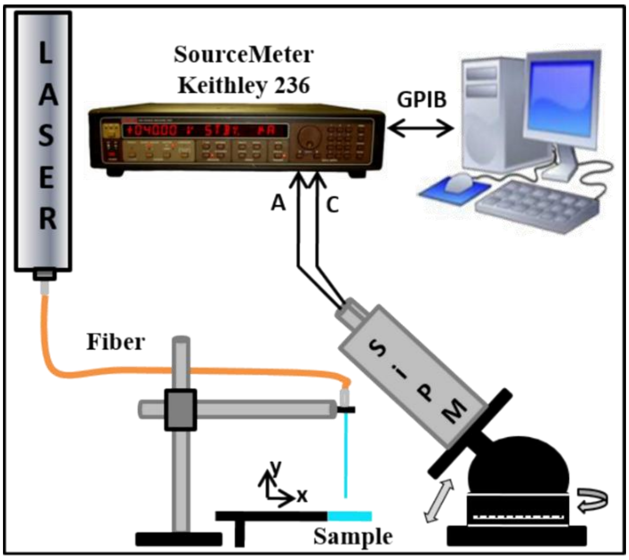

Figure 1: Measurement set-up.

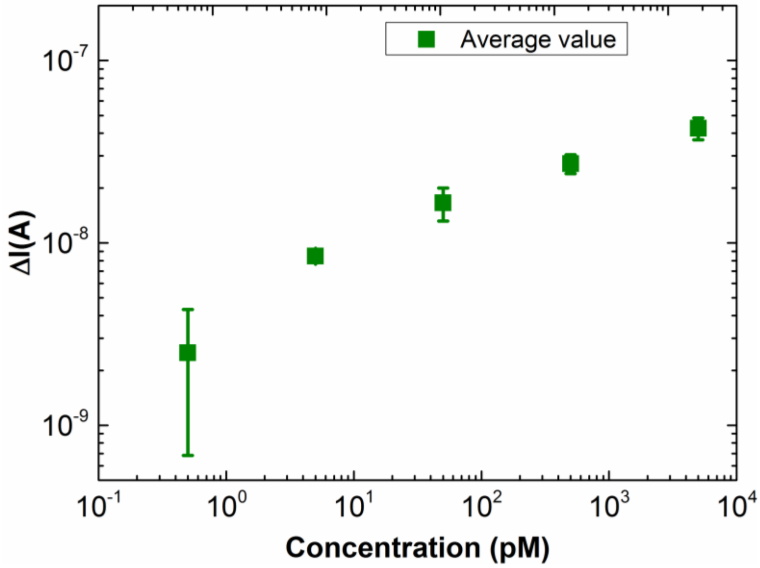

Figure 2: Detected fluorescence current changing FAM concentration.

Structural Health Monitoring System Using a Flexible Piezopolymer Transducers Array

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This work describes the characteristics and experiments of an acousto-ultrasonic Structural Health Monitoring System (SHM) for real-time active and passive mode detection of potential damaging events, e.g.: random impacts during launch; identify the structure integrity status during space missions operation cycle in order to allow the residual structure life prediction, finally reducing maintenance and increasing composite re-usability. The system exploits an innovative flexible piezopolymer transducers array instrumentation. The SHM has been developed within the project Program STEPS2 co-founded by EU.

The test article is a Full Scale Carbon Fiber Overwrapped Pressure Vessel (COPV) to carry pressuring gas on space missions. COPV is composed of an aluminum metallic liner and a filament winding carbon fiber reinforced polymer (CFRP) external shell. The low-profile low mass ultrasonic transducers array is permanently and rigidly glued to the COPV surface using a space qualified epoxy adhesive. The transducers are a custom design based on piezo-polymer film technology with interdigital electrode patterns (IDT) [1],[2].

A total of 16 IDTs are arranged in two linear arrays having 8 elements each. The arrays use a flex circuit interconnect made of Polyimide having different functions: to minimize the encumbrance of the transducer assembly, to simplify integration-verification phases and finally to reduce mass due to harness reduction (see Fig. 1).

The main electronics boards of the SHM system [1] are:16 analog front-end electronic boards, one per transducer manufactured by CORONA Spa; the commercials boards TI AFE5851 EVM, 12-bit, 16-channel VGA running at 20MSps and Xilinx SP605 Spartan 6 (see Fig. 2).

The principal SHM system diagnostic mode goals is initially to detect any potential and random impact event [2] during manufacturing or service life triggering an active mode to damage detection scan (using a custom damage detection algorithm equipped on an host PC) and deliver as final output a numerical index of system integrity.

The SHM instrumentation has been developed initially on laboratory and later SHM technology demonstration has been carried out on Thales Alenia Space Italia - Turin facilities (TAS-I). The impact campaign on full scale test article consisted on four impacts (#1,#2,#3,#4) with characteristics and positions shown in Table 1 and Fig. 1.

An impact result example is shown in Fig. 3, illustrating the damage graphical view produced by a high energy impact. In conclusion the system successfully reached its main goals addressing future technology development aimed to space flight application where University of Florence and STEPS2 partners are involved.

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Impact test #	Energy [J]	Real position [mm]	Estimated position [mm]
1	7	x=240; y=50	x=237; y=94
2	30	x=180; y=130	x=176; y=91
3	30	x=390; y=50	x=333; y=104
4	30	x=290; y=90	x=279; y=82

Table 1: Test impact positions and energy levels. Table also shows the estimated positions of all impacts

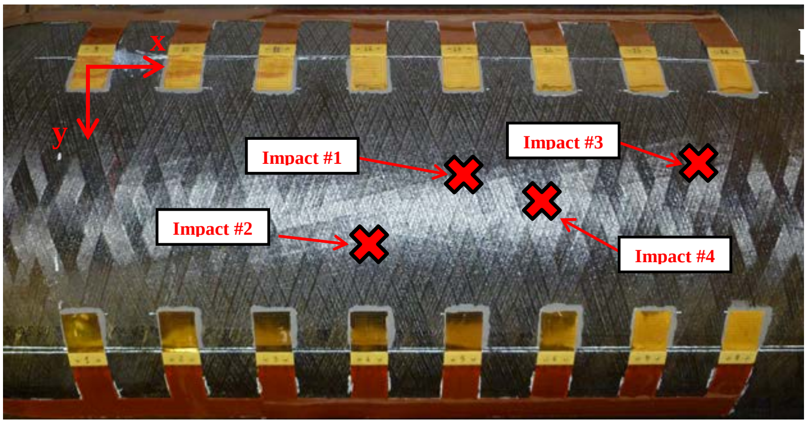

Figure 1: COPV monitored area and impact positions. a) transmitting array. b) receiving array

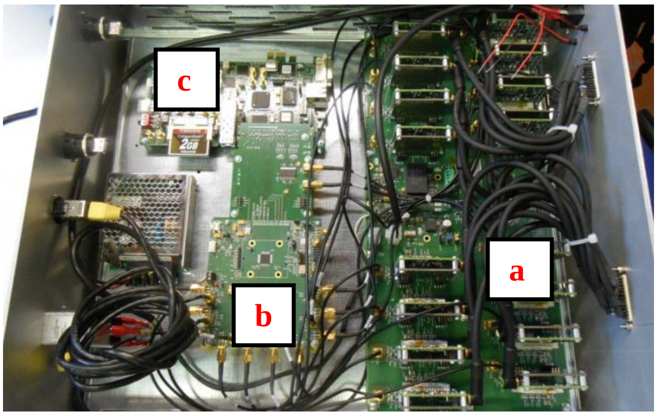

Figure 2: The main electronics boards of the SHM system. a) 16 analog front-end electronic boards; b) TI AFE5851 EVM; c) Xilinx SP605 Spartan 6

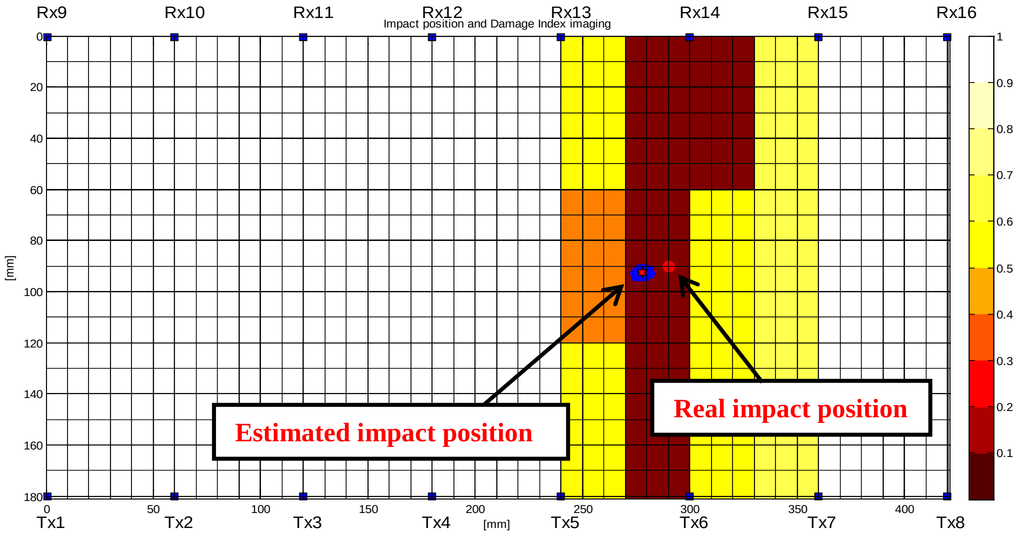

Figure 3: Damage Index colormap and position of impact #4

Testing the Accuracy of an Interface for Quasi-digital sensors

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The following work describes the results obtained by testing an alternative frequency to digital converter oriented to quasi-digital sensor interfaces. The problem with high resolution conversion is among the top priorities in electronics.

Conventional ADCs at the state of the art present the following characteristics: up to 32-bit resolution and a sample rate that is an integer multiple of common data rates for communication standards (common sample rates of 78.6 MSPS, 92.16 MSPS, 122.88 MSPS, and 245.76 MSPS).

Voltage-to-frequency converters (VFCs) consists of first-order oscillators: the input is an analog voltage V_i and the output is a frequency signal f_0 linearly proportional with m to the input signal, $f_0=mV_i$.

In this work we study a VFCs system which works as a part of an analog-to-digital converter to be integrated in an interface circuit (endowed with a embedded microcontroller) for sensor signal treatment. In this context a quasi-digital converter is used to digitize the sensor output signal (also exploiting microcontroller functions) and realizing the final conversion timed by its internal clocks.The converter here tested (the UFDC-1) [1] utilizes a novel frequency-time conversion method which allows it to maintain a programmable relative error from 1 to 0.001% in all specified ranges of frequencies for either frequency or period measurement [2].

In this work authors show what percentage error was recorded for each frequency given as input. Using a dedicated conversion protocol (the interface is able to operate with different duty cycle set-ups) an effective counteraction of the noise due to the sensors output signal can be performed.All figures were experimentally obtained utilizing the mode FX1 mode [2]. The input was given to the indicated pin [2], labeled as ‘FAST’. In particular, the input for all the measure-tests was a square signal with a 5 volt amplitude and offset of 2.5 volts. The tested accuracies are 1%, 0.1%, 0.01%, 0.001%. For every input five values were recorded per accuracy. The frequency values tested are the following: 0.05, 0.5, 5, 50, 500, 5000, 50000, 100000, 500000, 1000000, 2000000 Hertz. The percentage error is shown in figure 1. The mean measured outputs for the Accuracy level of 0.001% are reported in Table 1. These results confirm the performance claimed by the application note. Besides, the characteristic curves evidenced by the %error reported in figure 1, suggest that error trend could be studied and fitted in order to shape the converter behaviour in different functioning conditions thus to allow an optimal and adaptive re-calibration of its working parameters depending on the different experimental conditions of the sensor interfaced by the UFDC-1.

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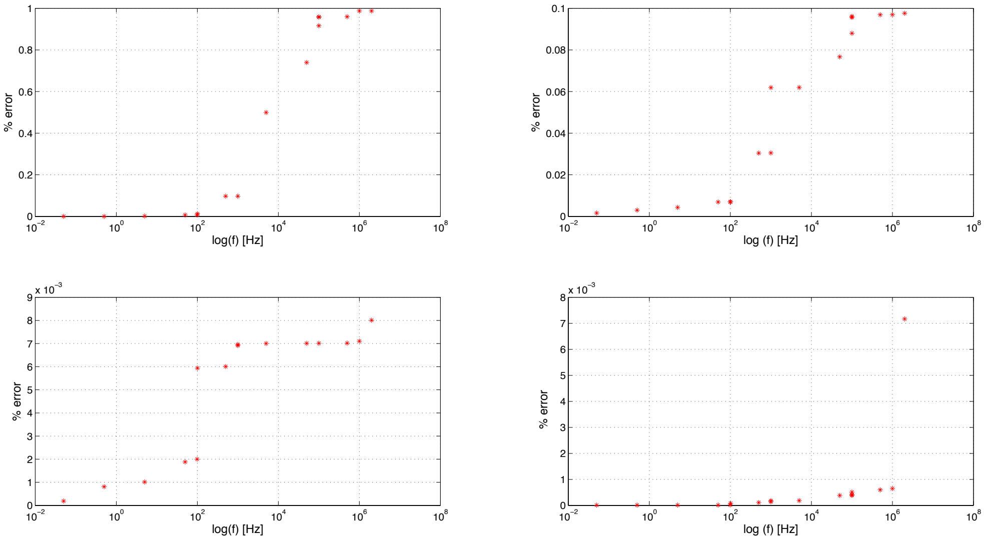

Figure 1: % error vs log(f) at four different set-ups

Table 1: average frequency registered for each input

Input frequency [Hz]	Mean value of the five outputs [Hz]
0.05	0.050003584
0.5	0.500001918
5	4.999990628
50	50.00032444
500	499.999914
5 K	5000.000475
50 K	49999.93011
100 K	100000.0124
500 K	500000.0618
1 M	1000005.124
2 M	2000008.247